DOI: 10.3969/j. issn. 1673-5188. 2016. S1. 004
http://www.cnki.net/kcms/detail/34.1294.TN.20161221.1058.002.html, published online December 21, 2016

Low-Power High-Efficiency Multi-Gigabit 60 GHz Transceiver Systems Routing in Vehicular Environments

Chul Woo Byeon[1] **and Chul Soon Park**[2]
(1. Department of Electronic Engineering, Wonkwang University, Iksan 54538, Korea;
2. Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea)

Abstract

This paper proposes low-power high-efficiency multi-gigabit 60 GHz transceiver systems for short-range communications. 60 GHz multi-gigabit on-off keying (OOK) receiver system-in-package (SiP) module is developed using a low temperature co-fired ceramic (LTCC) technology. Integrated with a low-power complementary metal oxide semiconductor (CMOS) OOK demodulator, the LTCC receiver module demonstrates Full-HD uncompressed video streaming at a distance of 1 m. A low-power and high-efficiency fully integrated OOK transceiver is also developed to be integrated in a handheld device. The transceiver consumes 67 mW at 10.7 Gb/s and occupies an active footprint of 0.44 mm^2. With an on-board Yagi-Uda antenna, the transceiver achieves 10.7 Gb/s of data transmission, resulting in a high energy efficiency of 6.26 pJ/bit. The antenna-in-package module with the transceiver demonstrates mobile-to-display 1080p Full-HD video transmission over a distance of 60 cm.

Keywords

60 GHz; Transceiver; on-off keying (OOK); Multi-gigabit

1 Introduction

In response to the demand for higher data rates, the millimeter-wave (mm-wave) band has been studied. Among the mm-wave bands, the 60 GHz band has been widely researched to achieve multi-gigabit data transmission [1]–[12]. The studies on a silicon-based 60 GHz band have demonstrated multi-gigabit wireless data transmission, which confirms the possibility of removing all high speed wire lines. With the 60 GHz band, we can surely remove wires of the signal lines and wirelessly connect all devices such as smart phones, laptops, displays, and tablet PCs. However, the transceivers in [1]–[3] consume a huge amount of DC power, which limits the use of mobile devices because of their limited battery capacity. The transceivers in [4]–[6] consume a low amount of DC power, but they support a limited communication distance of less than 20 mm.

This paper presents an overview of the low-power high-efficiency multi-gigabit 60 GHz transceiver systems. The proposed work simultaneously meets the requirements of the power and transmission distance budgets. This paper is organized as follows. Section 2 describes the low-power, high-efficiency 60 GHz multi-gigabit complementary metal oxide semiconductor (CMOS) solutions. Section 3 describes a 60 GHz multi-gigabit on-off keying (OOK) transmit/receive module integrated with a low-power CMOS OOK demodulator and GaAs chips. Section 4 presents a low-power high-efficiency transceiver module with an on-board antenna. Finally, this paper concludes with a summary in Section 5.

This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) grant funded by the Korean Government (MEST) (No. R11-2005-029-05001-0), the Institute for Information & communications Technology Promotion (IITP) grant funded by the Korea government (MSIP) (13-911-04-007), and the National Research Foundation of Korea (NRF-2014R1A2A1A11054107).

2 60 GHz Multi-Gigabit CMOS Solutions

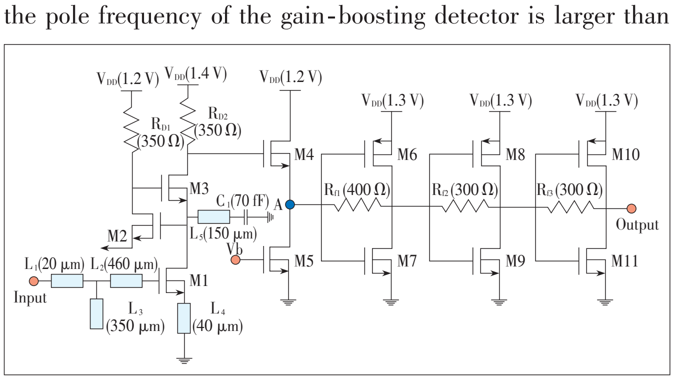
OOK modulation is one of the promising candidates for the short-range wireless communications due to its high integrity, simplicity, and low-power consumption. Several studies investigated the OOK modulation using silicon-based technologies [4]–[10]. The OOK transmitter simultaneously sends a data signal and a local carrier signal, and the OOK receiver detects the data using the local carrier signal from the transmitter. With this principle, the transmitter and receiver require no phase-lock alignment and the architecture and design are simplified.

The transceiver in [4] presents the basic architecture of the OOK system. The amplitude modulation was implemented by an up-conversion mixer, and the modulated signal was amplified by a power amplifier. Similarly, the transmitters in [5], [6], [13], [14], and [15] modulated the signal using an up-conversion mixer and amplified the modulated signal using a power amplifier. The up-conversion mixer as an OOK modulator has a high conversion loss, which causes high power dissipation to obtain a target transmit power at the transmitter. Therefore, the OOK transceiver systems are limited by the transmission distance or DC power dissipation. In the receiver, a detector without a phased-locked oscillator also has a high conversion loss [4], [14]. To overcome the high conversion loss of the detector, the receivers described in [5] and [6] added an injection path for the injection-locked oscillator. The injection-locked oscillator improved conversion gain, but the additional gain stage and oscillator consumed huge DC power, and the sensitivity of the injection-locked oscillator limited the receiver sensitivity. Alternatively, the receiver in [13] recovered the signal at an intermediate frequency but enhanced the gain and sensitivity of the detector at the cost of high DC power.

To overcome these drawbacks, we introduce a gain-boosting demodulator [9], a switching amplifier type of modulator, and a high-efficiency transmitter [8].

2.1 Highly Efficient Gain-Boosting Demodulator

To substitute the injection-locked oscillator [5], [6], the detector should have a high conversion gain for lower DC power and better sensitivity and wider bandwidth for high data rate. Therefore, the gain-boosting demodulator was introduced. A schematic of the 60 GHz gain-boosting OOK demodulator in 0.13 μm CMOS is shown in **Fig. 1**. The gain-boosting stage, M2-M3, contributes higher conversion gain while the conventional detector only uses M1 and has limited gain and bandwidth characteristics. The voltage conversion gain of the gain-boosting detector is $1+A$ times greater than the voltage conversion gain of a conventional detector, where A is the gain from the common source of M2. The dominant pole frequency of the gain-boosting detector is $1/((C_{D3}+C_L)R_{03})$, where R_{03} is the output resistance at the drain of M3, while dominant pole frequency of the conventional detector is $1/((C_{D1}+C_L)R_{03})$. C_{D1} is much larger than C_{D3} for larger conversion gain (higher gm2); thus, the pole frequency of the gain-boosting detector is larger than one of the conventional detectors. A resistive feedback inverter type amplifier is added after the 60 GHz OOK detector for high output voltage.

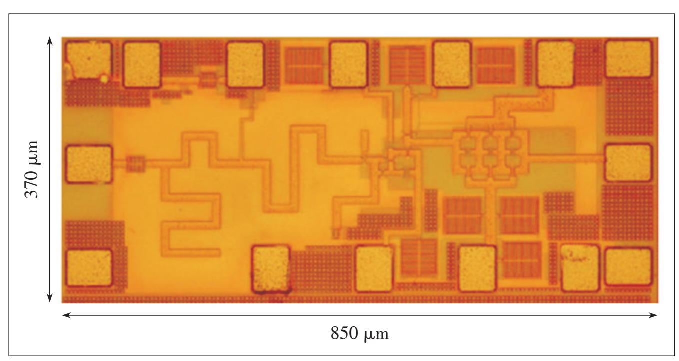


▲Figure 1. 60 GHz gain-boosting OOK demodulator schematic.

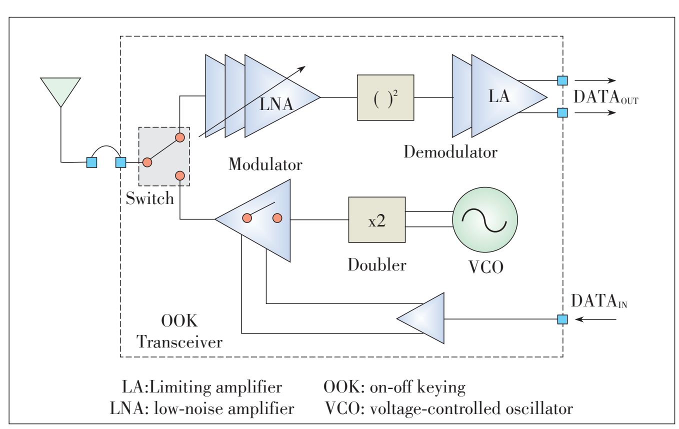
A microphotograph of the fabricated demodulator is shown in **Fig. 2** The demodulator consumes a small chip area of 0.32 mm^2 and a low DC power of 14 mW. With the gain-boosting technique, the detector has a voltage responsivity of 2434 mV/mW and the demodulator has a conversion gain of 13.6 dB at an input power of -16 dBm. The demodulator possesses a data capability of 5 Gb/s. Thus, an energy efficiency of 2.94 pJ/bit is achieved.

2.2 Low Power and Highly Efficient OOK Transceiver

Future wireless connectivity will require low power consumption, a high data rate, and short-range data transmission. To meet those requirements, a gain-boosting demodulator, a switching amplifier type of modulator, and a high-efficiency transmitter were introduced in [8]. We fabricated and demonstrated a low power and highly efficient OOK transceiver in 90 nm CMOS. **Fig. 3** shows a block diagram of the transceiver. The required signal-to-noise ratio of 10^{-12} bit error rate (BER) for OOK modulation is approximately 17 dB. A noise figure of 9 dB in the Rx is assumed. The required output power of the Tx is 5 dBm with antenna gain of 7 dBi over a distance of 30 cm at a data rate of 3.5 Gb/s. And the Rx sensitivity is -49 dBm. The transmitter consists of an OOK modulator, a dou-



▲Figure 2. 60 GHz gain-boosting OOK demodulator microphotograph.



▲Figure 3. 60 GHz transceiver block diagram.

bler, and a 30 GHz voltage-controlled oscillator (VCO). The modulator provides high output power and a modulation function. Futhermore, the modulator consumes DC power only in the data-on state, which results in a huge reduction in DC power consumption. The modulator has a gain of 9.1 dB in the on-state and a gain of -15.2 dB in the off-state; hence, it has an on/off isolation of 24.3 dB at 60 GHz. The output 1 dB compression point is 5.1 dBm with power-added efficiency of 12.7% at 60 GHz. To further reduce the DC power consumption and enhance the efficiency, the frequency doubler is directly attached to the 30 GHz VCO. The local oscillator (30 GHz VCO + frequency doubler) generates an output power of -0.9 dBm at 60 GHz. The on-state transmitter has an output power of 4.4 dBm with 8.9% power efficiency, including the switch loss.

The receiver consists of a low-noise amplifier (LNA) and a demodulator. To achieve a high data rate and high efficiency, we designed the LNA to have a wide bandwidth, low-noise figure, and high gain. The LNA has gains of 24.5 dB (high gain mode) and 15.5 dB (low gain mode) at 60 GHz with a 3 dB bandwidth of 14 GHz. A noise figure of 4.9 dB–6 dB is attained for the high gain mode. The demodulator adopts a gain-boosting technique and consists of a limiting amplifier and a detector. The detector has a voltage responsivity of 5892 mV/mW at 5 Gb/s and the limiting amplifier has a gain of 21.7 dB with a 3 dB bandwidth of 3.5 GHz. A die photograph of the transceiver is shown in **Fig. 4**. The transmit/receive switch is integrated for a small package size.

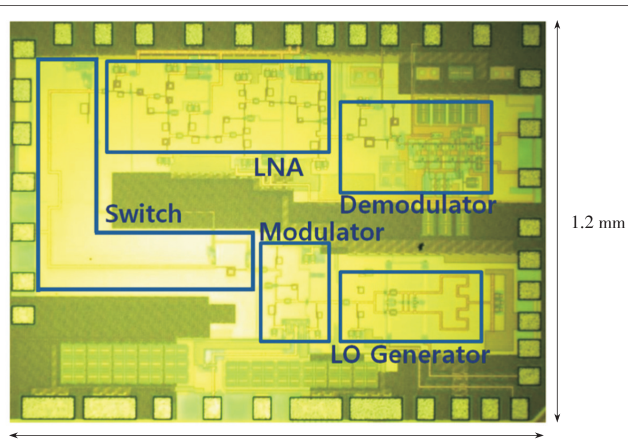
3 60 GHz Multi-Gigabit Transmit/Receive Modules

Multi-layer low-temperature co-fired ceramic (LTCC) technology is widely used due to its low-attenuation, low cost, similar value of temperature coefficient of expansion, and high integration capability to multi-/single-chip solutions [13]. **Fig. 5** shows the LTCC system-in-package (SiP) receiver and transmitter modules. The LTCC has a relative permittivity and a loss tangent of 5.8 and 0.0035, respectively. The size of the entire SiP with five ceramic layers is 37mm x 11mm x 0.5mm and 25.5mm x 10.5mm x 0.5mm for Tx and Rx, respectively. The radiating patches are placed on the top layer, and feeding network is located on the second layer while the ground plane is on the back side of the third layer. The antenna, fed by the bondwire and with the T-network for bondwire compensation, radiates through the coplanar waveguide with the ground to the embedded micro-strip line. The T-network consists of inductor, wide width transmission line (capacitor) and narrow width transmission line (inductor). The receiver and transmitter modules have a 1 by 2 patch antenna and a single patch antenna, respectively. The antennas have a simulated gain of 9.8 dBi and 4.8 dBi and a half power beamwidth of 100° and 60°, respectively. The transmitter module is integrated with a 30 GHz VCO, a frequency doubler, an up-conversion mixer, a drive amplifier, and a power amplifier. The receiver module is integrated with an LNA and the gain boosting demodulator in Fig. 2.

For multi-gigabit data transmission, we tested the fabricated modules. **Fig. 6** shows a demonstration of the multi-gigabit video signal transmission. Video data of 1.485 Gb/s is transmitted at a distance of 1 m.

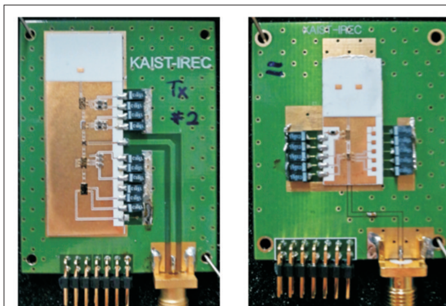
4 Highly Efficient 60 GHz Transceiver Module

An on-board antenna is one of the best candidates consider-



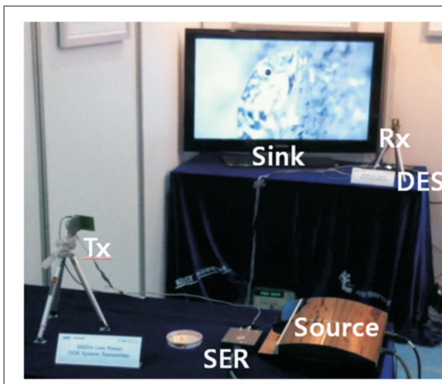
LNA: low-noise amplifier LO: local oscillator

▲Figure 4. 60 GHz transceiver chip microphotograph.



(a) (b)

Figure 5. 60 GHz system-in-package (SiP): (a) transmitter and (b) receiver.



DES: Deserializer SER: Serializer

Figure 6. Demonstration of multi-gigabit video signal transmission.

ing yield and cost. In this design, we use a Taconic substrate for the antenna design. The substrate has a dielectric constant of 3 and a thickness of 0.13 mm. A Yagi-Uda antenna [16] is used for high gain and end-fire radiation. The fabricated antenna size is 4 mm X 9 mm. **Fig. 7** shows the simulated radiation pattern of the antenna and the 60 GHz transceiver module with the high-efficiency CMOS transceiver and external bias circuitry in Fig. 4. The fabricated antenna is directly attached next to the CMOS transceiver chip on the PCB. The 60 GHz signal is connected to the antenna through two parallel gold wires with an approximate length of 300 μm, and their parasitic inductance is resonated out using a matching network on the antenna. The antenna has a simulated gain of 9.8 dBi. The beamwidth for E-plane and H-plane is 48° and 60°, respectively.

The measurement performance and wireless video signal transmission of the transceiver module are depicted in **Fig. 8**. A data rate of 10.7 Gb/s was achieved over a distance of 6 cm with a BER less than 10^{-12} for the 2^7-1 pseudorandom binary sequence (PRBS). Also, data rates of 5 Gb/s were observed over distances of 40 cm with a BER of less than 10^{-12}. **Table 1** compares this work with previously published works. This work shows the lowest energy efficiency of 6.26 pJ/bit with a high data rate of 10.7 Gb/s and a low power consumption of 67 mW. The 60 GHz transmitter module sends Full-HD data from a mobile phone to a display through the 60 GHz receiver module. Video data of 2.97 Gb/s is transmitted a distance of 60 cm.

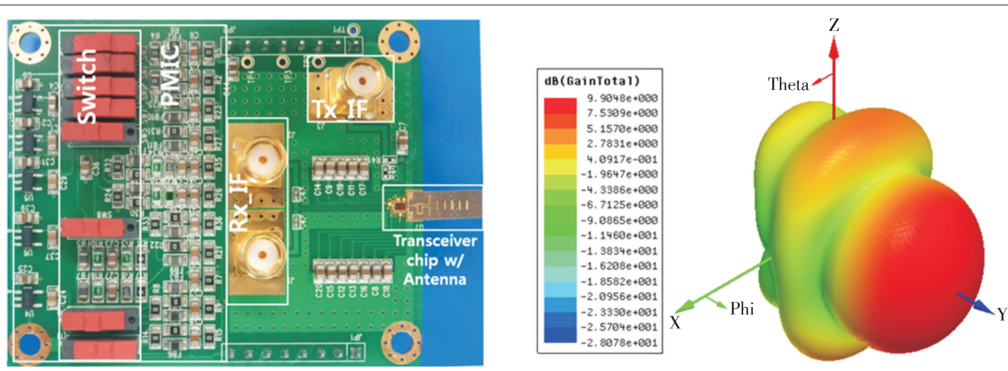
5 Conclusions

This paper presents low-power high-efficiency multi-gigabit 60 GHz transceiver systems. For a highly efficient design, we develop a gain-boosting demodulator and a highly integrated low-power transceiver in a CMOS technology, which can handle multi-gigabit data transmission faster than 5 Gb/s. We develop the 60 GHz multi-gigabit LTCC receiver module with the low-power CMOS OOK demodulator and demonstrate multi-gigabit (1.485 Gb/s) video data transmission. Futhermore, to be integrated in a handheld device, the antenna-in-package module with the transceiver demonstrates mobile-to-display 1080p (2.97 Gb/s) wireless Full-HD video transmission over a distance of 60 cm.

References

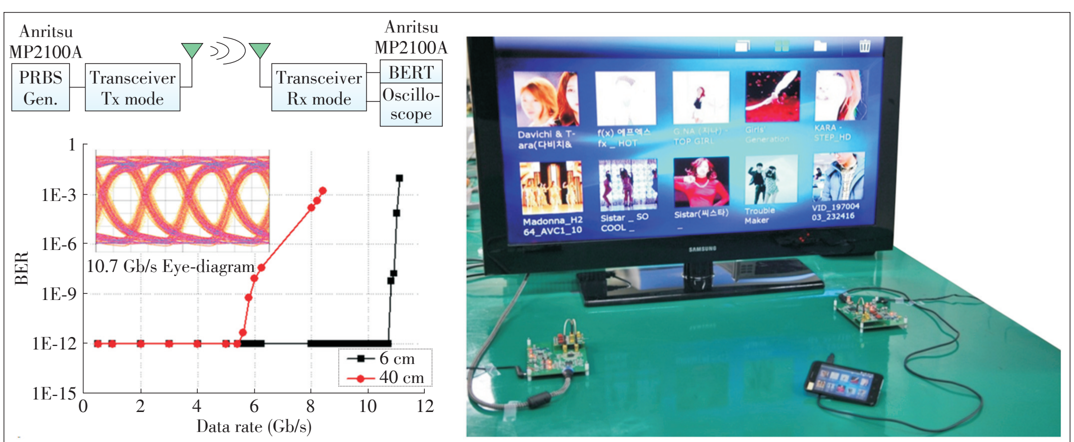
[1] M. Boers "A 16TX/16RX 60 GHz 802.11ad chipset with single coaxial interface and polarization diversity," in *IEEE International Solid-State Circuits Conference*, San Francisco, USA, Feb. 2014, pp. 344–345. doi: 10.1109/ISSCC.2014.6757462.

[2] A. Tomkins, et al., "A 60 GHz, 802.11ad/WiGig-Compliant Transceiver for Infrastructure and Mobile Applications in 130 nm SiGe BiCMOS," *IEEE Journal of*



IF: Intermediate frequency PMIC: Power management integrated circuit

Figure 7. Photograph of 60 GHz transceiver module and simulated radiation pattern of the antenna.



BER: bit error rate BERT: bit error rate tester PRBS: pseudorandom binary sequence

Figure 8. Measured transceiver performance and demonstration of multi-gigabit (Full-HD) video signal transmission.

Table 1. Performance comparison

References	[14]	[5]	[6]	[17]	[18]	This work
Technology	90 nm CMOS	40 nm CMOS	40 nm CMOS	45 nm SOI CMOS	65 nm CMOS	90 nm CMOS
Carrier frequency	60 GHz	57 GHz	57/80 GHz	60 GHz	60 GHz	60 GHz
Modulation	OOK	ASK	ASK	BPSK	16QAM	OOK
Power dissipation	286 mW	70 mW	137 mW	317 mW	542 mW	67 mW
Switch	No	No	No	No	No	Yes
Tx/PA P_{1dB}	5 dBm (PA)	-2 dBm (Tx)	-15.2/-9.5 dBm (Tx)	15 dBm (Tx)	6 dBm (Tx)	5.1 dBm (PA) 4.4 dBm (Tx)*
Tx efficiency (P_{OUT}/P_{DC})	1.73 %	2.18 %	0.27 %	15.3 %	1.3 %	8.9 %**
Rx sensitivity	-30 dBm***	-33 dBm***	-	-	-35 dBm***	-32.5 dBm
Data rate	2.5 Gb/s	11 Gb/s	20 Gb/s	5 Gb/s	7 Gb/s	10.7 Gb/s
Distance	40 mm	14 mm	5 mm	loopback	300 mm	100 mm
EE	114 pJ/bit	6.4 pJ/bit	6.85 pJ/bit	63.4 pJ/bit	77.4 pJ/bit	6.26 pJ/bit
Chip area	Tx: 0.43 mm^2 Rx: 0.68 mm^2	Tx: 0.06 mm^2 Rx: 0.07 mm^2	Tx: 0.16 mm^2 Rx: 0.26 mm^2	4.42 mm^2	5.48 mm^2	Tx: 0.15 mm^2 Rx: 0.29 mm^2

*: Tx output power including switch
**: Including switch
***: Calculated from table
ASK: amplitude-shift keying
BPSK: binary phase shift keying
CMOS: complementary metal oxide semiconductor
EE: energy efficiency
OOK: on-off keying
PA: Power Amplifier
QAM: quadrature amplitude modulator
SOI: silicon on insulator

Solid-State Cicuits, vol. 50, no. 10, pp. 2239–2255, Oct. 2015. doi: 10.1109/JSSC.2015.2436900.

[3] K. Okada "A 64-QAM 60 GHz CMOS transceiver with 4-channel bonding," in *IEEE International Solid-State Circuits Conference*, San Francisco, USA, Feb. 2014, pp. 346–347. doi: 10.1109/ISSCC.2014.6757463.

[4] W. Chen, S. Joo, S. Sayilir, et al., "A 6-Gb/s wireless inter-chip data link using 43-GHz transceivers and bond-wire antennas," *IEEE Journal of Solid-State Cicuits*, vol. 44, no. 10, pp. 2711– 2721, Oct. 2009. doi: 10.1109/JSSC.2009.2027932.

[5] K. Kawasaki, Y. Akiyama, K. Komori, et al., "A millimeterwave intra-connect solution," *IEEE ISSCC Digest of Technical Papers*, Feb. 2010, pp. 414–415. doi: 10.1109/ISSCC.2010.5433831.

[6] Y. Tanaka, Y. Hino, Y. Okada, et al., "A Versatile Multi-Modality Serial Link," *IEEE ISSCC Digest of Technical Papers*, Feb. 2012, pp. 332–333. doi: 10.1109/ISSCC.2012.6177034.

[7] C. Byeon, et al., "A 60-GHz transceiver system with low-power CMOS OOK modulator and demodulator," in *IEEE International Microwave Workshop Series on Intelligent Radio for Future Personal Terminals (IMWS-IRFPT)*, Daejeon, Korea (South), Aug. 2011, pp. 100–101. doi: 10.1109/IMWS2.2011.6027205.

[8] C. Byeon, C. Yoon, and C. Park, "A 67-mW 10.7-Gb/s 60-GHz OOK CMOS transceiver for short-range wireless communications," *IEEE Transaction on Microwave Theory and Techniques*, vol. 61, no. 9, pp.3391–3401, Sept. 2013. doi: 10.1109/TMTT.2013.2274962.

[9] C. Byeon, J. J. Lee, K. Eun, and C. S. Park, "A 60 GHz 5 Gb/s Gain-boosting OOK Demodulator in 0.13μm CMOS," *IEEE Microwave and Wireless Components Letters*, vol.21, no.2, pp. 101– 103, Feb. 2011. doi: 10.1109/LMWC.2010.2096411.

[10] J. J. Lee and C. Park, "A 60 GHz Gbps OOK Modulator with High Output Power in 90nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 5, pp. 249– 253, May 2011. doi: 10.1109/TCSII.2011.2124890.

[11] C. Byeon and C. S. Park, "Design and Analysis of the Millimeter-wave SPDT Switch for TDD Applications," *IEEE Transaction on Microwave Theory and Techniques* , vol. 61, no. 8, pp. 2258–2864, Aug. 2013. doi: 10.1109/TMTT.2013.2271613.

[12] C. Byeon, J. J. Lee, I. Song, and C. S. Park, "A 60 GHz Current-Reuse LO-Boosting Mixer in 90 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol.22, no.3, pp. 135– 137, Mar. 2012. doi: 10.1109/LMWC.2011.2182636.

[13] I. S. Song, et al., "A low loss 60GHz radio integrating CMOS circuits with LTCC AiP," in *Proc. 2011 IEEE EDAPS*, Hangzhou, China, pp. 1–4. doi: 10.1109/EDAPS.2011.6213757.

[14] Jri Lee, Yenlin Huang, Yentso Chen, Hsinchia Lu, and Chiajung Chang, "A Low-Power Fully Integrated 60GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly," *IEEE ISSCC Digest of Technical Papers*, Feb. 2009, pp. 316–317,317a. doi: 10.1109/ISSCC.2009.4977435.

[15] E. Juntunen, et al., "A 60-GHz 38-pJ/b 3.5-Gb/s 90 nm CMOS OOK digital radio," *IEEE Transaction on Microwave Theory and Techniques*, vol. 58, no. 2, pp. 348–355, Feb. 2010. doi: 10.1109/TMTT.2009.2037867.

[16] H. Yagi, "Beam transmission of the ultra short waves," *Proc. IRE*, vol. 16, pp. 715–741, Jun. 1928. doi: 10.1109/JRPROC.1928.221464.

[17] T. Dinc, A. Chakrabarti, and H. Krishnaswamy, "A 60 GHz CMOS Full-Duplex Transceiver and Link with Polarization-Based Antenna and RF Cancellation," *IEEE Journal of Solid-State Cicuits*, vol. 51, no. 5, pp. 1125–1140, May 2016. doi: 10.1109/JSSC.2015.2507367.

[18] K. Okada, et al., "Full four-channel 6.3-Gb/s 60-GHz CMOS transceiver with low-power analog and digital baseband circuitry," *IEEE Journal of Solid-State Cicuits*, vol. 48, no. 1, pp. 46–65, Jan. 2013. doi: 10.1109/JSSC.2012.2218066.

Manuscript received: 2016-06-15

Biographies

Chul Woo Byeon (cwbyeon@wku.ac.kr) received the PhD degree in electronic engineering from Korea Advanced Institute of Science and Technology (KAIST), Korea, in 2013. During 2013, he was a postdoctoral researcher with the Department of Electrical and Computer Engineering from University of California, San Diego, USA. From 2014 to August 2015, he was a senior engineer with Samsung DMC R&D Center, Korea, where he was involved in developing a millimeter-wave/RF transceiver for 5G cellular communications. In September 2015, he joined the Department of Electronic Engineering, Wonkwang University, Korea, where he is currently an assistant professor. His research interests include CMOS/SiGe millimeter-wave/RF integrated circuits, antennas, packages, and system design for wireless communications.

Chul Soon Park (c-spark@kaist.ac.kr) received the BS degree from Seoul National University, Korea in 1980, and the MS and PhD degrees in materials science and engineering from the KAIST in 1982 and 1985, respectively. From 1985 to 1999, he was with the Electronics and Telecommunication Research Institute (ETRI), Korea, where he contributed to the development of semiconductor devices and circuits. From 1987 to 1989, he studied the very initial growth of group IV semiconductors for laser applications during a visit to AT&T Bell Laboratories, USA. Since 1999, he has been with the Information and Communications University (which merged with KAIST in 2009), where he is a full professor with the Engineering School. His research interests include reconfigurable RF integrated circuits (RFICs), millimeter-wave integrated circuits (ICs), and their system-on-chip (SoC)/system-on-package (SoP) integration.