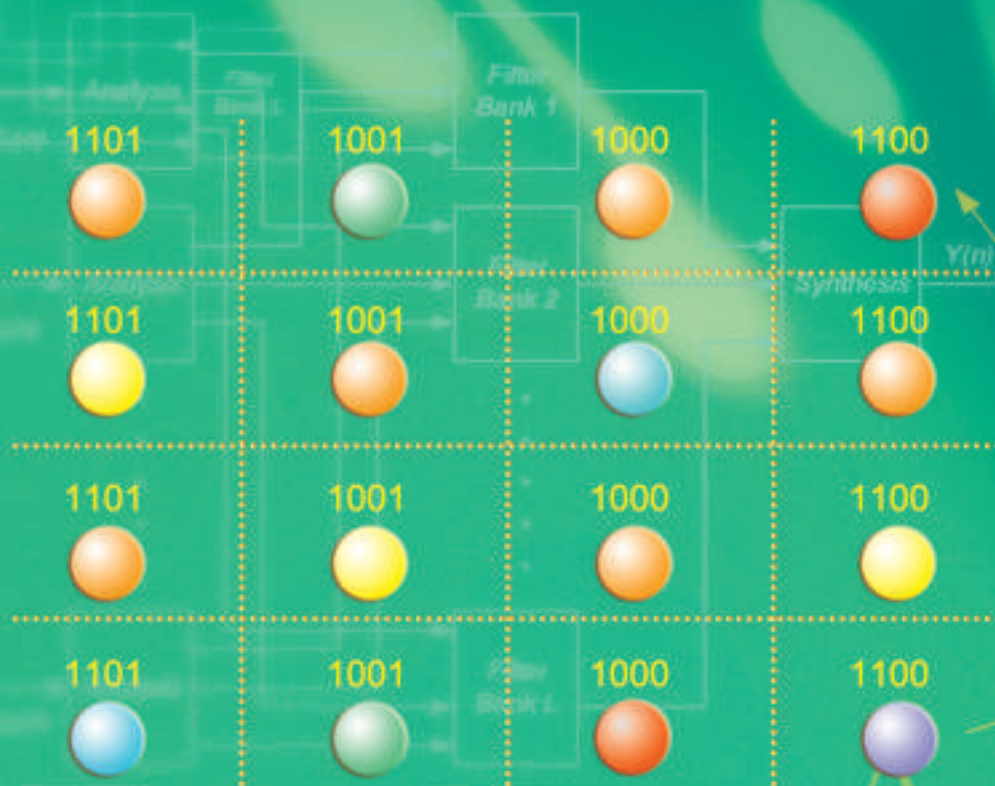


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Special Topics:

Advances in Digital Front-End and Software RF Processing: Part II
Advances in Mobile Data Communications



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Frost & Sullivan Recognizes ZTE as 2011 LTE Vendor of the Year



ZTE Corporation announced on November 10, 2011 that it has been named LTE Vendor of the Year by leading consulting firm Frost & Sullivan.

The Frost & Sullivan LTE Vendor of the Year award is given to companies that have achieved excellence in LTE. ZTE won the award for its growing number of secured contracts and also for its patent applications. The company's industry leading equipment has entered high-end markets such as Europe, Japan, and the

United States. ZTE is one of the world's most competitive LTE solutions providers.

ZTE's influence in the global LTE market has steadily grown. In first half 2011, the number of new LTE contracts exceeded the total number of LTE contracts for the whole of 2010. ZTE has won 28 contracts for LTE commercial application and has deployed test networks in conjunction with more than 90 operators worldwide. To date, more than 100,000 ZTE LTE terminal units have been ordered worldwide. The terminals, which are purchased by high-end operators, contribute to the commercialization of LTE technology.

"ZTE is honored to be recognized by Frost & Sullivan as a leader in the LTE field," said Mr. Richard Lihe Ye, the senior director of wireless product operation for ZTE Corporation. "The award illustrates the company's commitment to the development and commercialization of next-generation technology."

ZTE is a leader in developing LTE technologies. To date, ZTE has applied to ETSI for 235 essential patents for LTE standards, accounting for approximately 7 per cent of the total number of EP applications globally. (ZTE Corporation)

ZTE Becomes Global Leader in CDMA Base Station Market with 33% Share

ZTE Corporation announced on November 3, 2011 that it has become the global leader in the CDMA base station market, with a 32.6 percent share in first half 2011.

According to a recent IDC analytical report on the global CDMA market, ZTE has increased its shipments of CDMA base stations steadily in recent years. As of the end of first half of 2011, the company's shipment of base-stations had exceeded 320 thousand units, pushing it to the top spot in the global CDMA base station market.

ZTE is the first company in the telecom industry to introduce a CDMA/LTE dual-mode system. This innovative CDMA/LTE product can assist operators to smoothly upgrade their existing networks to future networks and faster evolve to LTE systems. This solution, along with the company's EV-DO Rev. B system, is recognized as industry leading.

The global CDMA market has grown in recent years, especially in Asia Pacific, where it has expanded rapidly. Coupled with a loss in market share by several established North American CDMA suppliers, this has prompted ZTE to seek new opportunities in CDMA markets across the globe. Through these efforts, the

company has acquired a leading market share in emerging nations such as, China, Indonesia, and India. It also has achieved significant breakthroughs in North America.

IDC Analyst John Byrne believes that "ZTE is the leader of the global CDMA market and will be in the strongest position in emerging global markets, as been the case in the global CDMA market. ZTE will continue to create greater value for operators."

As of the end of first half 2011, ZTE's CDMA products have been put into large-scale commercial use by more than 120 operators in more than 70 countries worldwide. The company has built more than 80 CDMA2000 1xEV-DO networks in 60 countries and regions including the Czech Republic, India, Indonesia, and the United States in the same period. In addition, ZTE has won 23 contracts for commercial application of LTE solutions from operators including CSL, Telenor, Sonaecom, and H3G and has deployed LTE test networks in conjunction with more than 80 operators across the globe. To date, ZTE has received orders for more than 100,000 LTE terminals from several leading global operators. (ZTE Corporation)

ZTE Establishes Global Consumer Brand Ambitions in 2011

ZTE Corporation became the fourth largest handset vendor by market share in 2011 and set out its ambitions for further growth with a series of high-profile celebrity sponsorship deals.

According to a Q3 report by ABI research, IDC, and Strategy Analytics, ZTE overtook Apple to become the fourth-largest handset manufacturer in the world. According to the report, ZTE shipped 19.1 million terminals in Q3 2011, a 57.9 percent increase year on year. ZTE's market share also increased to 4.9 percent, which closed the gap between ZTE and 3rd place, LG Electronics. In the first three quarters of 2011, ZTE's revenue from terminal sales increased 53.4 percent year on year.

ZTE is not resting on its laurels and is looking forward to 2012. Backed by strong financial and business performance, ZTE will invest more in marketing initiatives next year to bring its brand recognition in line with its global market share.

In April, ZTE announced its smart terminal strategy, part of which included partnering with the Singaporean singer/songwriter, Huang Yida, to create the new brand song "Light Your Smart World," which is also ZTE's smart terminal slogan.

In May, ZTE unveiled the new Light Pro tablet at the Mutua Madrid Open, an ATP World Tour Masters 1000 event, with support from Spanish PR Agency, Perception & Image. The device included an application specifically designed for the tournament. The application provided statistics, player information, and match schedules in real time. The world's top tennis player, Carlos Moyà Llompart, was also invited to experience ZTE's smart terminal products.

In September, ZTE launched its flagship smartphone, Skate, during Cibeles Madrid Fashion Week. Spanish supermodel, Jon Kortajarena, presented ZTE products at the event, further strengthening the company's brand. In Hong Kong, the Skate launch was endorsed by local pop star, Kandy Wong with support from Edelman Hong Kong.

In October, ZTE, in conjunction with PR agency, AxiCom, announced an exclusive deal with EMI Music/Virgin Records to sponsor leading UK rapper, Professor Green, on an 18 day UK tour. The campaign includes an ongoing Twitter competition @ZTE_UK for



SIM-free Skate terminals, a ticket give-away supported by local media, and an integrated Facebook campaign on facebook.com/ZTEUK. Professor Green fans had the opportunity to win free tickets to an exclusive London gig and some very lucky fans to meet the performer face-to-face.

Also in October, ZTE announced the exclusive sponsorship of Spanish artist, David Bisbal's, tour 'Acustico'. The tour started on November 1 with a special concert in the Teatro Real in Madrid. This sponsorship package is part of ZTE's marketing strategy for the launch of ZTE Skate.

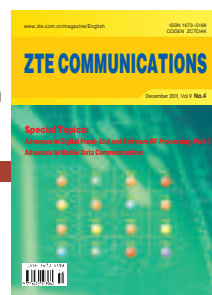
ZTE also secured exclusive sponsorship of all the handsets in China's top-rated TV series, "Man's Gang." ZTE presents its full series of smartphones and tablets in the TV series, strengthening ZTE's smart terminal brand with fashion-conscious youth.

"ZTE has been involved in a wide range of celebrity and entertainment marketing campaigns over the past 12 months, marking 2011 as a watershed year in the company's transition from white label ODM to fully fledged own-brand player," said He Shiyu, head of ZTE's mobile-terminals business. "Next year looks set to be even bigger and brighter, as we continue on our roadmap to becoming a top-three handset player by the year 2015."

(ZTE Corporation)

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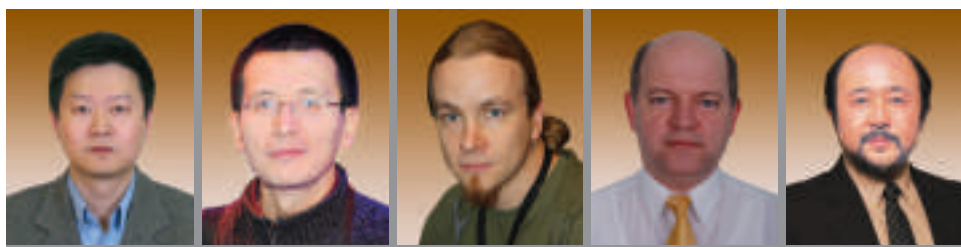
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Advances in Digital Front-End and Software RF Processing: Part II



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In the first editorial of this two-part special issue, we pointed out that one of the biggest trends in wireless broadband, radar, sonar, and broadcasting technology is software RF processing and digital front-end [1]. This trend encompasses signal processing algorithms and integrated circuit design and includes digital pre-distortion (DPD), conversions between digital and analog signals, digital up-conversion (DUC), digital down-conversion (DDC), DC offset, and I/Q imbalance calibration. Other important related topics are peak-to-average power ratio (PAPR) reduction, crest-factor reduction (CFR), pulse shaping, image rejection, digital mixing, delay/gain imbalance compensation, error correction, noise shaping, numerical-controlled oscillator (NCO), and various diversity methods. Digital techniques for RF processing have many advantages over traditional techniques in terms of power efficiency, cost and area reduction, flexibility, programmability, and reconfigurability. Digital RF processing is now regarded as key to enabling software-defined radio (SDR) that supports multistandard, multimode applications and fast time-to-market solutions [2], [3].

This special issue aims to stimulate and guide the development of new and improved systems for wireless communications and digital broadcasting. It is a timely and high-quality forum for scientists, engineers, technologists, broadcasters, manufacturers, software developers, and other professionals to engage in discussion. In this special issue of *ZTE Communications* published in English, we wish to show how the theory is translated into practical technology for all the relevant standards. Readers are given ideal design methodologies to manage a rapidly increasing range of applications.

Step-by-step information for designing practical systems is included, and theory, principles, algorithms, standards, and implementation are all given comprehensive treatment.

The call-for-papers for this special issue attracted a good number of excellent submissions. After two-round reviews, twelve papers have been selected for publication in this

special issue, which is organized into two parts and has been published in two consecutive issues in 2011.

The contents of part I is divided into two groups. The first group consists of four papers, addressing different aspects of power amplification (PA) technologies. The second group, comprising two papers, is devoted to another interesting topic: architecture design and test of millimeter wave (60 GHz) wideband radio transceivers, which are mainly based on a six-port device and related technology. For more details on this part, refer to [1].

Six papers have been selected for publication in part II, and these papers are organized again into two groups. The first group consists of three papers that focus on theory, design, and implementation of resampling, that is, up-conversion and down-conversion. The second group consists of three papers that describe non-uniform channelization of multiplexed frequency bands, selective subcarrier degradation-based crest-factor reduction, and an eigenfiltering-based antenna diversity scheme.

The first paper by Mehmood Awan, Yannick Le Moullec, Peter Koch, and Fred Harris describes efficient processing engines in the digital radio front-end. These engines, based on a polyphase channelizer, perform arbitrary sample-rate changes, frequency selection, and bandwidth control. The polyphase filter bank with five different resampling modes is used as a case study for embedded resampling in digital front-ends. These modes are (i) maximally decimated, (ii) under-decimated, (iii) over-decimated, and combined up- and down-sampling with (iv) single stride length and (v) multiple stride lengths. These modes can be used to obtain any required rational sampling rate change in an SDR front-end based on a polyphase channelizer. They can also be used for translation to and from arbitrary center frequencies that are unrelated to the output sample rates. In a future issue, the authors will report on their work analyzing hardware architecture of polyphase channelization.

The paper by Yue Zhang, Li-Ke Huang, Carsten Maple and Qing Xuan gives an overview of the concepts, theory, and

design principles of digital down-conversion and up-conversion for SDR-based communication and broadcasting systems. After an introduction to essential concepts and principles, the paper discusses design issues in down-conversion, and super-heterodyne and direct-conversion architectures are presented. Details of the SDR design for up-conversion are described in this paper, and trade-offs in the design stages for filters, mixers, NCO, DAC, and signal processing are discussed in detail.

In the third paper of the first group, Álvaro Palomo Navarro, Rudi Villing, and Ronan Farrell deal with the practical implementation of two non-uniform channelization techniques for multiplexed frequency bands. These techniques are based on generalized DFT filter banks (GDFT-FB), which are a major processing task in the receivers of an SDR system. Filter bank-based schemes are efficient and flexible; however, the use of FIR filters generally leads to high filter orders, and this is impractical. To overcome this problem, a multistage filtering structure is applied to the GDFT-FB to reduce the number of coefficients. In this approach, the number of filter coefficients and operations per input sample is less than that in the single-stage approach. These reductions make fixed-point implementation using existing FPGA platforms more practical.

In the second group of papers, the first paper by R. Neil Braithwaite deals with crest-factor reduction. Selected data subcarriers are modified within an OFDM signal to reduce peaks in the time domain, and pilot and null subcarriers remain unchanged. In this approach, a set of peaks within an OFDM symbol interval are identified, and data subcarriers whose data element has a positive or negative correlation to the peak set are selected. For a subcarrier with an outer element and significant positive correlation, a bit error (reversal) is intentionally introduced in order to move the data element to the opposite side of the constellation. Outer elements on negatively-correlated subcarriers are increased in magnitude along the real or imaginary axis. Simulations described in this paper show that selecting the correct subcarriers for bit reversals and outward enhancements reduces the peak-to-average power ratio of the OFDM signal to a target value. At the same time, in-band degradation caused by bit error rate (BER) is limited.

In the paper by Fa-Long Luo, Ward Williams, and Bruce Gladstone a new antenna diversity system is proposed that uses eigenfiltering for OFDM-based wireless communication and digital broadcasting applications. Compared with the existing schemes, such as post-FFT, pre-FFT, and polyphase-based filter-banks, the proposed scheme performs optimally and has very low computational complexity. The adaptive algorithm for updating the eigenfiltering coefficients has the same complexity as the LMS algorithm. The proposed scheme offers a better compromise between performance, power consumption, and complexity in the real-time implementation of receivers in broadband communication and digital broadcasting systems.

The last paper in this special issue deals with analog-to-digital conversion and describes a histogram approach to error correction. The paper by Armin Jalili, J.

Jacob Wikner, Sayed Masoud Sayedi and Rasoul Dehghani describes a static calibration technique for flash analog-to-digital converters (ADC). The calibration technique is based on histogram test methods, and estimation of the equivalent errors in the flash ADC comparators is done in the digital domain, without any significant changes being made to the ADC comparators. In the trimming process, the reference voltages are adjusted to compensate for static errors. Behavioral-level simulations of a moderate-resolution 8-bit flash ADC show that, for typical errors, ADC performance is considerably improved by the proposed technique. Implementation of the proposed technique will be discussed in a future issue.

We would like to thank again all authors for their valuable contributions. We also express our sincere gratitude to all the reviewers for their timely and insightful comments on all submitted papers. It is hoped the content of this two-part special issue is informative and useful from various technological and implementation perspectives.

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Biographies

Jun Fang graduated from Shanghai Jiao Tong University in 1982 and received his Ph.D. from Ecole Nationale Supérieure des Télécommunications de Paris (ENST Paris) in 1987. He has been an associate professor at Shanghai Jiao Tong University since 1987. He worked with Alcatel Space Industries from 1990 to 2001 in several R&D and management positions. He was senior vice president of Linkair Communications USA from 2001 to 2005 and then worked as digital design director with TechnoConcepts from 2005 to 2006. During this time, he was involved in digital RF-mixed chip projects. Dr. Fang held a senior wireless system position in EDA with Cadence USA during 2006. Since 2009, he has been director of the Electronics & Information Technology Center of the Research Institute of Tsinghua University (RITS) and has led R&D and industrialization activities in wireless, signal processing, EDA, and digital TV multimedia. He has also been involved in wireless activities with CARITS Inc., a subsidiary of RITS in the U.S. Dr. Fang has written one book on information theory and coding, and he has contributed to ITU publications on satellite systems. He has 10 patents and published many technical papers. His research interests include SDR, digital RF chip design, and MIMO transmission systems.

Fa-Long Luo is chief scientist at two leading international companies headquartered in Silicon Valley, CA, that deal with SDR and wireless multimedia. He has been the editor-in-chief of the *International Journal of Digital Multimedia Broadcasting* since 2007. Dr. Luo is currently chairman of the IEEE Industry DSP Standing Committee and technical board member of the IEEE Signal Processing Society. He has 28 years of research and industrial experience in multimedia, communication and broadcasting with real-time implementation, applications, and standardization. He has received worldwide recognition. Dr. Luo has authored and edited four books, more than 100 technical papers, and 18 patents on these and closely related fields.

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Polyphase Filter Banks for Embedded Sample Rate Changes in Digital Radio Front-Ends

Mehmood Awan¹, Yannick Le Moullec¹, Peter Koch¹, and Fred Harris²

1. Technology Platforms Section, Dept. of Electronic Systems, Aalborg University, Denmark;

2. Dept. of Electrical & Computer Engineering, San Diego State University, CA, USA)

Abstract: This paper presents efficient processing engines for software-defined radio (SDR) front-ends. These engines, based on a polyphase channelizer, perform arbitrary sample-rate changes, frequency selection, and bandwidth control. This paper presents an M-path polyphase filter bank based on a modified N-path polyphase filter. Such a system allows resampling by arbitrary ratios while performing baseband aliasing from center frequencies at Nyquist zones that are not multiples of the output sample rate. This resampling technique is based on sliding cyclic data load interacting with cyclic-shifted coefficients. A non-maximally-decimated polyphase filter bank (where the number of data loads is not equal to the number of M subfilters) processes M subfilters in a time period that is less than or greater than the M data loads. A polyphase filter bank with five different resampling modes is used as a case study for embedded resampling in SDR front-ends. These modes are (i) maximally decimated, (ii) under-decimated, (iii) over-decimated, and combined up- and down-sampling with (iv) single stride length, and (v) multiple stride lengths. These modes can be used to obtain any required rational sampling rate change in an SDR front-end based on a polyphase channelizer. They can also be used for translation to and from arbitrary center frequencies that are unrelated to the output sample rates.

Keywords: SDR; digital front-ends; polyphase filter bank; embedded resampling

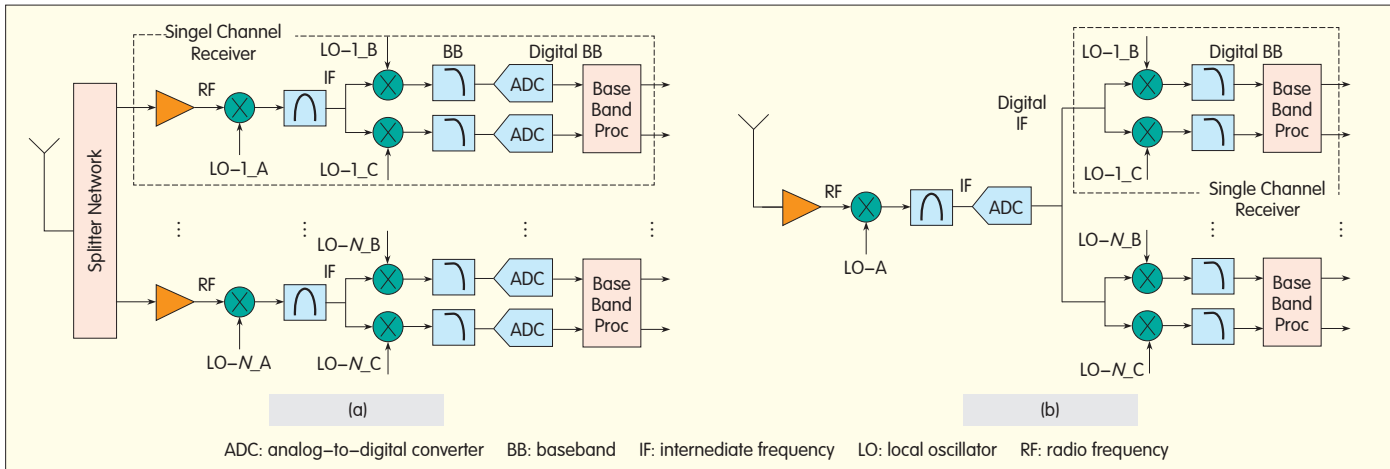
1 Motivation

There are several generations of architectures for digital radio transceivers. A base station in a cellular mobile communication system is an example of a multichannel radio receiver that simultaneously down-converts and demodulates narrowband radio frequency (RF) channels [1], [2]. Traditional heterodyne architecture, considered the first generation of digital radio architecture, is shown in Fig. 1(a) for an N -channel receiver. Each subreceiver consists of a dual-stage down-converter, and only the baseband processing is done in the digital domain [2]. In the first stage, the RF signal is down-converted to bandlimited intermediate frequency

(IF). In the second stage, the IF filter output is again down-converted to baseband by a matched-quadrature mixer and matched baseband filters that perform final bandwidth control. Next, the signal passes into the digital domain where the output of the analog-to-digital converter (ADC) is processed by digital signal processing (DSP) engines. These engines perform the required baseband processing, that is, synchronization, equalization, demodulation, detection, and decoding. The problem with this type of architecture is that amplitude and phase are imbalanced. This results in cross-talk between the narrowband channels because of aging (time, temperature) of the analog components of the quadrature down-converter. Each imbalance-related spectral

image must be lower than the desired spectral term, and this is difficult to sustain over time and at varying temperatures.

The need for extreme I/Q balance gave rise to the next generation of radios where second-stage (IF) down-conversion and, consequently, the channelization process are digitized, as shown in Fig. 1(b). Digital conversion at IF provides greater control over the imbalance by manipulating the number of bits involved in the arithmetic operation. The precision of the coefficients used in the filtering process sets an upper limit for spectral artifacts at -5 dB/bit. This means that a 12-bit ADC can achieve image levels below -60 dB [2]. DSP-based complex down-conversion, however, has two



▲ Figure 1. (a) First generation of digital radio architecture for an N-channel receiver, and (b) Second generation of digital radio architecture for an N-channel receiver.

advantages: the spectral images are controlled so that they are below the quantization noise floor of the ADC involved in the conversion process, and the digital filters before and after the mixers are designed to have linear phase characteristics [2]. The second generation of radio, with digital front-end, is a realizable version of SDR. The range of applications for second-generation architecture, shown in Fig. 1(b), is restricted to those with IF center frequencies of a couple of hundred megahertz. This is due to the limited dynamic range of high-speed ADCs. The dynamic range is often extended by using a hybrid scheme in which the initial complex down-conversion is performed by analog I/Q mixers, and channelization is performed digitally after the ADC. DSP techniques are applied to the digitized I/Q data to balance the gain and phase offsets in the analog ADC [3].

A digital front-end with a standard design that includes frequency selection, bandwidth reduction, and sample rate reduction is one of the most power- and time-critical functionalities of an SDR terminal. This is due to the large bandwidth and high dynamic range of the signal to be processed. Consequently, the digital signals may have high sample rates and large word lengths. High sample rates not only increase power consumption but also make the use of time-shared hardware infeasible [4]. On the other hand,

multirate signal processing specifies new ways of performing DSP tasks, and these ways are not normally available in traditional DSP designs. A multirate polyphase filter can perform the tasks of a multichannel receiver. In such a receiver, an input signal is composed of many equal-bandwidth, equally spaced frequency-division-multiplexed (FDM) channels. These channels are digitally down-converted to baseband (bandwidth is constrained by digital filters) and subjected to a sample rate reduction commensurate with the bandwidth reduction. This significantly reduces the number of system resources required to perform multichannel processing and, consequently, reduces costs [2], [3].

The remainder of this paper is organized as follows: In section 2, we briefly introduce a polyphase channelizer and describe how it is formulated from a conventional channelizer. In section 3, we categorize the embedded resampling cases described in [5] into five different resampling cases: maximally decimated, under-decimated, over-decimated, and combined up- and down-sampled with single and multiple commutator stride lengths. In section 4, we perform MatLab simulations and the simulation results demonstrate the performance of polyphase channelizers that deliver the targeted output sample rates. Section 5

concludes the paper.

2 Introduction

A multirate polyphase filter can perform the tasks of a multichannel receiver. These tasks are equivalent to down-conversion, filtering, and resampling of multiple narrowband signals [5]. The step-by-step conversion of a standard single-channel demodulator into a multichannel polyphase channelizer is described in [2] and [3]. A brief introduction is given here. In the standard single-channel demodulation process, shown in Fig. 2(a), the carrier-centered spectrum is translated to baseband (where a filter reduces the bandwidth), and a resampler reduces the sample rate in proportion to the bandwidth reduction. Standard single-channel demodulation is described by

$$y(n, k) = [x(n) e^{-j\theta_k n}] \times h(n) \quad (1)$$

$$y(n, k) = \sum_{r=0}^{N-1} x(n-r) e^{-j\theta_k(n-r)} h(r) \quad (2)$$

where $x(n)$ is the carrier-centered input signal, θ_k is carrier angular frequency for k th channel, $h(n)$ is the baseband filter, and $y(n, k)$ is the output baseband signal for k th channel.

According to the Equivalency Theorem [3], down-conversion followed by baseband filtering can be reordered so that filtering at the carrier occurs first, followed by

down-conversion. This is the opposite of the traditional channelization process. Fig. 2(b) shows this reordered operation, which is also described by

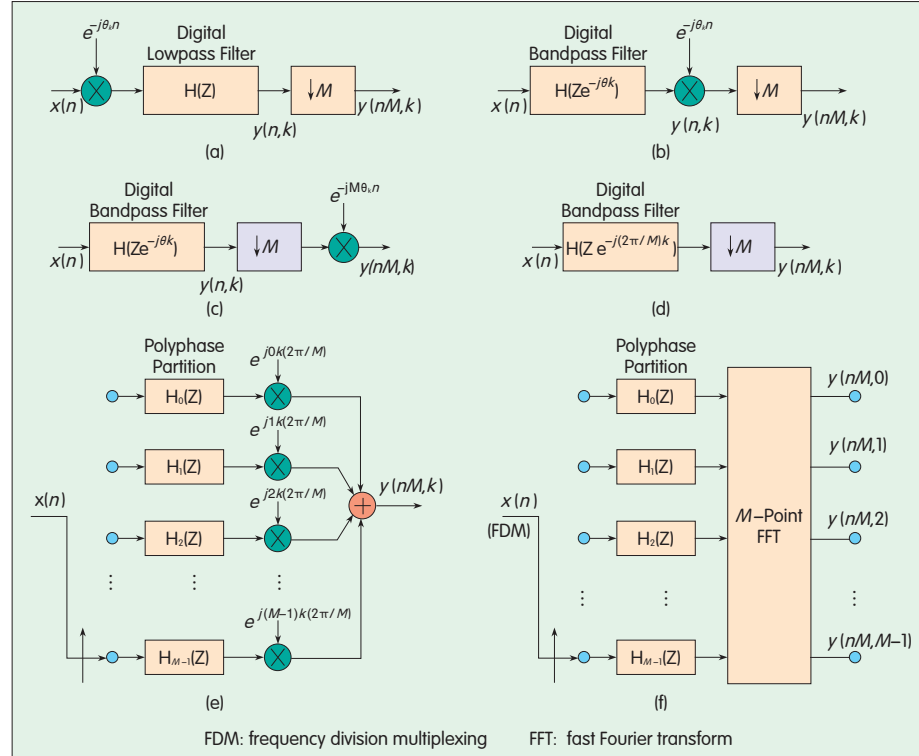
$$y(n, k) = e^{-j\theta_k n} \sum_{r=0}^{N-1} x(n-r)h(r) e^{-jr\theta_k} \quad (3)$$

To reduce the work involved in down-converting and then discarding the samples during resampling, the heterodyne and down-sampler are reordered, and only retained samples are down-converted, as shown in Fig. 2(c). In this case, the frequency of the heterodyne at the reduced sample rate is $M\theta_k$ rad/sample rather than the original frequency of θ_k . If the center frequency, θ_k , is a multiple of the output sample rate $2\pi/M$, that is, $k(2\pi/M)$, then the center frequency is aliased to 0 by M -to-1 resampling. Under this condition, the down-sampled heterodyne defaults to unity and can be discarded, as shown in Fig. 2(d).

For the computed output for each input, $M-1$ of these computed output samples are discarded by the down-sampler. To reduce this workload, the resampling and the filtering operations are reordered so that one output is computed for every M input sample. This is achieved by applying the Noble identity [3], which describes how a filter processing every M th input sample followed by an output M -to-1 down-sampler is equivalent to an input M -to-1 down-sampler followed by a filter processing every input sample. The original up-converted filter is partitioned to M subfilters that operate at the reduced output rate rather than the original input rate. The mathematical expressions in (4) describe the mapping of the filter's Z -transforms at the input rate to a sum of Z -transforms at the output rate:

$$\begin{aligned} G(Z) &= \sum_{n=0}^{N-1} h(n) e^{j\frac{2\pi}{M}kn} Z^{-n} \\ &= \sum_{r=0}^{M-1} \sum_{n=0}^{M-1} h(r+nM) e^{j\frac{2\pi}{M}k(r+nM)} Z^{-(r+nM)} \quad (4) \\ &= \sum_{r=0}^{M-1} Z^{-r} e^{j\frac{2\pi}{M}kr} \sum_{n=0}^{M-1} h(r+nM) Z^{-nM}. \end{aligned}$$

The phase rotators in each subfilter are constant for that subfilter. Fig. 2(e) shows the block diagram for (4). The output resampler is pulled to the input side of each filter stage by applying the



▲ Figure 2. Transformation of a standard single-channel channelizer into a polyphase channelizer with M channels: (a) heterodyning, filtering, and down-sampling for a standard channelizer, (b) reordered channelizer using Equivalency Theorem, (c) reordering of the resampler, (d) down-converter with center frequency at a multiple of output sample rate aliases to baseband by M -to-1 down-sampling, (e) single-channel polyphase channelizer, and (f) polyphase channelizer for M channels.

Noble identity. The input delay elements Z^{-r} and the resampler at each stage are replaced by a rotary switch called a commutator.

In the final step of forming the polyphase filter bank, the sum formed by the phase rotators is one output port of a discrete Fourier transform (DFT). The DFT can be implemented as a fast Fourier transform (FFT) to extract time samples of each narrowband process located at multiples of the output sample rate (that has been aliased to baseband by the resampler) [5]. This is shown in Fig. 2(f) and given by

$$y(nM, k) = \sum_{r=0}^{M-1} y_r(nM) e^{j\frac{2\pi}{M}kr} \quad (5)$$

The relationship between the sampling frequency, channel spacing, and number of channels for the polyphase channelizer is

$$f_s = N \cdot \Delta f \quad (6)$$

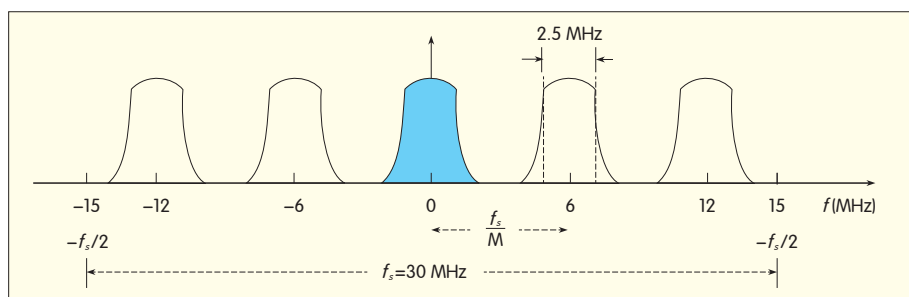
where f_s is the input sampling frequency, N is number of channels

(FFT size), which is the same as M here, and Δf is the inter-channel spacing [3].

The polyphase filter channelizer uses the input M -to-1 resampling to alias the spectral terms residing at multiples of the output sample rate to baseband. This means that for a standard polyphase channelizer processing M input samples at a time, the output sample rate is the same as the channel spacing. When operating in this mode, the system is a maximally decimated filter bank. We experimented with polyphase filter banks using embedded resampling and here present under-decimated, over-decimated, and combined up- and down-sampling (for single and multiple commutator stride lengths) modes.

3 Non-Maximally Decimated Filter Bank

We have briefly presented the polyphase filter bank channelizer in



▲ Figure 3. A 30 MHz FDM signal with 5 channels separated by 6 MHz center frequencies. Each channel has a 2.5 MHz symbol rate shaped by a square root Nyquist filter with 20% excess bandwidth.

which the output sample rate is the same as the channel spacing. However, in practice, an output sample rate that is different from the channel spacing is often required. To uncouple the output sample rate from the channel spacing, a straightforward approach is to resample each channel with P/Q resamplers [5]. By changing the values of P and Q, the required sample rate can be obtained. An alternative is to embed the resampling process in (i) the polyphase commutator, that is, in the interaction between input data registers and the polyphase coefficients, and in (ii) the interaction between the polyphase outputs and the FFT input. This alternative only requires a state machine to schedule the interactions, and there is no computational cost.

Two schemes [5] for these interactions are (i) serpentine shifting the input data that interacts with a fixed set of coefficients and circular buffering the filtered data prior to FFT, and (ii) sliding the cyclic data-load that interacts with cyclic-shifted coefficient memory. In the serpentine shift and circular buffering scheme, an input data set (not equal to M) is always fed to the same registers, and the polyphase subfilter coefficients are fixed. Let us consider a single-tapped delay line where all the data is moved further to the right before the next input data set is loaded. The data is moved by an address equal in length to the next input data set. By folding this one-dimensional tapped delay line into the two-dimensional memory of the polyphase filter, the data move is a serpentine shift between the columns. Because this non-equal M input data

set is loaded, the data time-origin moves with respect to the FFT time-origin. To keep these two origins aligned, the computed output of the polyphase filter is circular-shifted by the residue address of the data time-origin mod M before the FFT is performed. In the sliding cyclic data-load and cyclic shift of the coefficient memory scheme, the data registers are fixed instead of being cycled, and the coefficient sets are rotated. The input data is fed as sliding cyclic load by the input commutator to a fixed set of registers, and the subfilter coefficients are cyclic-shifted by the same residue address of the data time-origin mod M before FFT is performed. Taking individual subfilters into account, the first scheme seems to require more read and write operations to synthesize the serpentine data shift. However, this shift is, rather, achieved by circular wrapping of block memory (an address control task). In the second scheme, only the loading subfilter gets a data shift.

To demonstrate the embedded resampling, we here describe the example shown in Fig. 3. A system has 5 channels separated by 6 MHz center frequencies. Each channel has a 2.5 MHz symbol rate shaped by a square root Nyquist filter (with 20% excess bandwidth) to form a 30 MHz FDM channel. To satisfy the Nyquist criteria at the output sample rate, the output sample rate must be greater than the occupied channel bandwidth. The occupied channel bandwidth of 3 MHz (symbol rate plus excess bandwidth) is selected to be smaller than the channel bandwidth of 6 MHz to

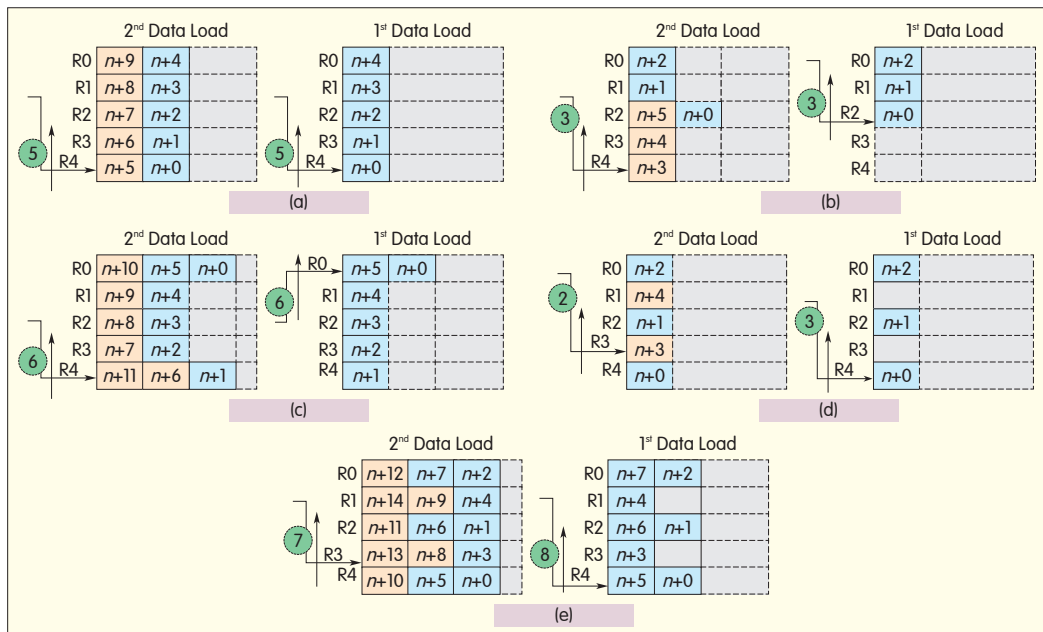
allow down-sampling by large factors within the channelizer. The down-sample channelizer uses a 30-tap prototype low-pass filter with around 60 dB side-lobe attenuation that is partitioned into a 5-path polyphase filter with 6-tap subfilters. Both the data bank and filter coefficient bank are two-dimensional memories of 5 rows and 6 columns, and each row corresponds to a subfilter. According to (6), the output sample rate for the maximally decimated system becomes 6 MHz, which is the same as the channel spacing. Four other resampling factors are also introduced, and two of these have an embedded up-sampling factor of two. These five resampling factors are 5, 3, 6, 5/2, and 15/2, delivering output sample rates of 6, 10, 5, 12 and 4 MHz, respectively. These correspond to maximally decimated, under-decimated, over-decimated, and combined up-and-down-sample cases. Each of these cases will be presented for the sliding cyclic data load and cyclic shift of the coefficient memory scheme.

Case 1: Maximally-Decimated Mode

In a maximally decimated system, data is loaded in stride lengths of 5 mod 5, and a computed output sample has a 5-to-1 down-sampling. Fig. 4(a) shows the data loading process for the two outputs. The subfilter's data register and coefficients are denoted R and C, respectively. In all the data loads, data loading starts from subfilter R4 up to R0, and the loaded subfilter's tapped delay line is pushed one tap to the right before a new data element is loaded. For every computed output, all the subfilters are fed with input data. Because there is no residue (non-loaded subfilter), there is no offset between the data time-origin and the FFT time-origin. The coefficients of the subfilters are therefore fixed from C0 to C4. There is only one state machine where the 5-point data-loading of the register bank always performs an inner product with the fixed set of subfilter coefficients. Table 1 shows the register loading sequence and corresponding subfilter coefficients.

Case 2: Under-Decimated Mode

In a non-maximally decimated



▲ Figure 4. Data loading processes for a 5-path polyphase filter performing (a) 5-to-1 down-sampling (case 1), (b) 3-to-1 down-sampling (case 2), (c) 6-to-1 down-sampling (case 3), (d) 5/2 down-sampling (case 4), and (e) 15/2 down-sampling (case 5).

▼ Table 1. Register loading sequence and corresponding subfilters coefficients for a 5-path maximally decimated system

State	Loading Sequence	Filter Coefficients
0	R4 R3 R2 R1 R0	C0 C1 C2 C3 C4

▼ Table 2. Register loading sequence and the corresponding subfilter coefficients for 3-to-1 sample rate change in a 5-path polyphase filter

State	Loading Sequence	Filter Coefficients
0	R2 R1 R0	C0 C1 C2 C3 C4
1	R4 R3 R2	C3 C4 C0 C1 C2
2	R1 R0 R4	C1 C2 C3 C4 C0
3	R3 R2 R1	C4 C0 C1 C2 C3
4	R0 R4 R3	C2 C3 C4 C0 C1

(under-decimated) system, data is loaded in stride lengths of $3 \bmod 5$, and a computed output sample has a 3-to-1 down-sampling within a 5-stage polyphase filter. The least common multiple (LCM) of 3 and 5 is 15, which means that the state engine cycles in 15 inputs, and because 3-point data is delivered at a time, there must be 5 distinct states in the state machine. Fig. 4(b) shows the data-loading processes for the first two

states.

In the first state, data loading starts from subfilter R2 up to R0; and in the second state, data loading starts from R4 to R2 and so on for the five distinct states. Consequently, there is a residue of 2 for each data-loading operation. To align the data time-origin with the FFT time-origin, the subfilter coefficients are cyclic-shifted by the residue address of the data time-origin mod 5. The time-origin that is being cyclically shifted is also periodic in the LCM of 3 and 5. Thus, the cyclic shift of the polyphase subfilter coefficients has the same period as the data register load and is controlled by the same state machine. The data-loading sequence is always to the next 3 registers that have indexing of mod 5, which means that the next register to accept data when moving from state 0 to state 1 is (R0)-1, which is actually R4. Similarly, the filter coefficients assigned to perform the inner products with the registers are always offset 3 mod 5 relative to the previous filter set. Table 2 shows the state machine for register-loading and coefficients of each corresponding subfilter for performing 3-to-1 down-sampling in a 5-stage polyphase filter.

Case 3: Over-Decimated Mode

In an over-decimated system, data is loaded in stride lengths of $6 \bmod 5$, and a computed output sample has a 6-to-1 down-sampling within a 5-stage polyphase filter. The LCM of 6 and 5 is 30, which means that the state engine cycles in 30 inputs, and because 6-point data is delivered at a time, there must be 5 distinct states in the state machine. Fig. 4(c) shows the data-loading processes for the first two states.

In the first data load, loading starts from subfilters R0, R4 up to R0, and the second load starts from R4 up to R0 and R4 again and so on for the 5 distinct

states. Consequently, there is a residue of 4 for each data-loading operation. To align the data time-origin with the FFT time-origin, the subfilter coefficients are cyclic-shifted by the residue address of the data time-origin mod 5. Table 3 shows the state machine for register-loading and the corresponding coefficients for performing 6-to-1 down-sampling in a 5-stage polyphase filter.

Case 4: Combined Up- and Down-Sampling Mode (Single Stride)

In the previous three cases, down-sampling was performed by different factors. The polyphase filter is also capable of embedding the up-sampling factor with the down-sampling so that the sample rate change is rational. In this case, we

▼ Table 3. Register loading sequence and the corresponding subfilter coefficients for 3-to-1 sample rate change in a 5-path polyphase filter

State	Loading Sequence	Filter Coefficients
0	R0 R4 R3 R2 R1 R0	C0 C1 C2 C3 C4
1	R4 R3 R2 R1 R0 R4	C1 C2 C3 C4 C0
2	R3 R2 R1 R0 R4 R3	C2 C3 C4 C0 C1
3	R2 R1 R0 R4 R3 R2	C3 C4 C0 C1 C2
4	R1 R0 R4 R3 R2 R1	C4 C0 C1 C2 C3

▼ Table 4. Register loading sequence and the corresponding subfilter coefficients for 5/2 sample rate change in a 5-path polyphase filter

State	No of Inputs	Loading Sequence	Filter Coefficients
0	3	R4 R2 R0	C0 C6 C2 C8 C4
1	2	R3 R1	C5 C1 C7 C3 C9

up-sample by a factor of 2 and then down-sample by a factor of 5 to obtain a 5/2 sample rate change. The up-sampling, performed by zero-packing the input data, is actually achieved by data-load addressing, in which one address is skipped so that 1-to-2 up-sampling can be realized. Down-sampling is performed by cyclic-loading the data (zero-packed) through the filter in stride of length 5. The two data-loading cycles for a 5/2 sample rate change in a 5-path polyphase filter are shown in Fig. 4(d).

In the first data load, 3 data samples are delivered to the 5 register addresses. In the second load, 2 data samples are delivered to the 5 register addresses. The data-loading process is periodic in 2 load cycles, and 2 states are needed to control the process. The data-loading process for the 2 states and the corresponding coefficient sets are listed in Table 4. In the 2 states, 5 inputs are delivered, and 2 outputs from the polyphase engine are taken to realize the desired 5/2 embedded resampling. The loading scheme has a constant offset of $-2 \bmod 5$ within a sequence and also in the transition between sequences. The -2 offset is a result of the 1-to-2 up-sampling, represented by the zero packing.

There are normally 5 subfilters in the polyphase partition of a 5-stage polyphase filter. Because of the 1-to-2 up-sampling implemented by the zero-packing, only half the coefficients in each stage actually contribute to the subfilter output [5]. Thus, each stage is further partitioned into 2 subsets of coefficients, which results in 10 subfilter coefficient sets. These sets are denoted C0, C1, ..., C9 where the integer is the starting index from the original non-partitioned prototype filter. The

successive filter index increments by 6 mod 10; and between the states, the filter index increments by 5 mod 10. The integer 6 is the offset between two data samples in the zero-packed load in two adjacent rows. Because of up-sampling by a factor of 2, the prototype filter has to be designed to operate at $2 \times f_s$, that is, 60 MHz. Consequently, the filter becomes twice as long as the standard design. However, because only half of it is used per processing cycle, there is no processing penalty [5].

Case 5: Combined Up- and Down-Sampling Mode (Multiple Strides)

This case is similar to case 4 but down-sampled by a factor of 15 to have a 15/2 sample rate change. Up-sampling is performed by data-load addressing, which skips the next address, and down-sampling is performed by cyclic-loading the data through the filter in stride lengths of 15. The two states of the loading cycle for 15/2 sample rate change in a 5-path polyphase filter are shown in Fig. 4(e).

In the first data load, 8 data samples are delivered to the 5 register addresses. In the second load, 7 data samples are delivered to the 5 register addresses. The data-loading process is periodic in 2 load cycles, and 2 states are needed to control the process. Table 5 lists the data-loading process for the 2 states and the corresponding coefficient sets. In the process, 15-to-2 down-sampling is performed in a 5-path polyphase filter. The filter down-converts the spectral regions from multiples of $f_s/5$ (or $30/5 = 6$ MHz) and maintains a sample rate of $f_s(2/15)$ (or $60/15 = 4$ MHz).

4 Simulations

The MatLab simulations show the embedded sample rate changes in a 5-path polyphase filter and DFT operating as a 5-channel channelizer. The FDM input signal has 5 channels that are each 16-QAM modulated and separated by 6 MHz center frequencies. The sample rate

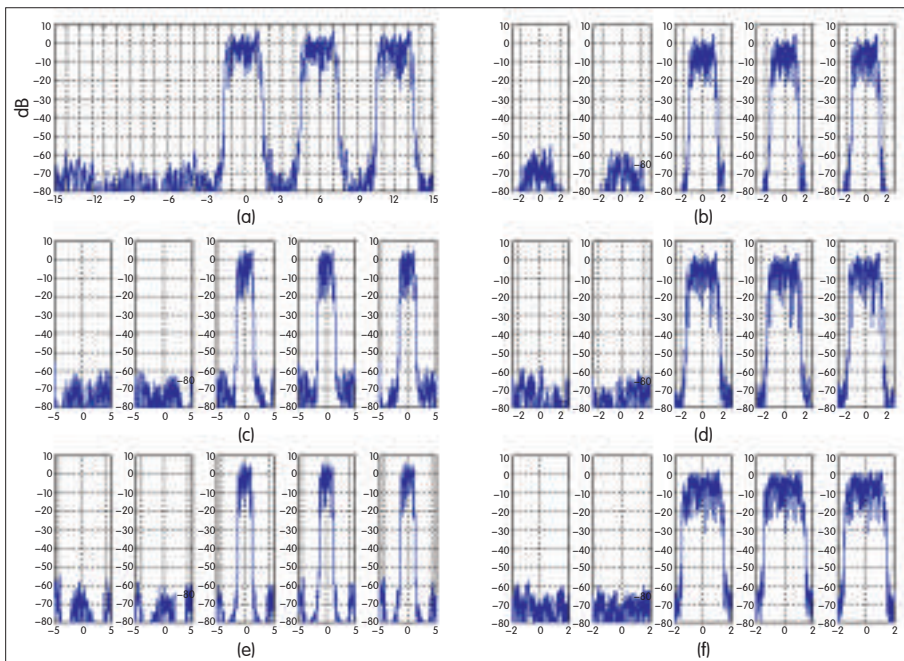
is 30 MHz, and each channel has a 2.5 MHz symbol rate shaped by a square root Nyquist filter with 20% excess bandwidth. Three of the five channels, which are occupied by 3 MHz bandwidth signals, are centered at 0, 6, and 12 MHz. The remaining two channels, centered at -12 and -6 MHz, are intentionally kept empty. The input signal spectrum comprising 5 channels at 30 MHz is shown in Fig. 5(a).

In a system operating in maximally decimated mode, the input data is channelized and down-sampled 5-to-1 for an output rate of 6 MHz. Each of the 5 polyphase filter stages are 6 taps long and are anchored to the 5 input registers being fed by the periodic input commutator. Fig. 5(b) shows the spectra of the 5 output channels with an output rate of 6 MHz. In a system operating in under-decimated mode, the same input data is channelized and down-sampled 3-to-1 for an output rate of 10 MHz. Fig. 5(c) shows the spectra of the 5 output channels with 10 MHz output rate. Similarly, in a system operating in over-decimated mode, the same input data is channelized and down-sampled 6-to-1 for an output rate of 5 MHz. Figure 5(d) shows the spectra of the 5 output channels with 5 MHz output rate.

In a system operating in combined up- and down-sampling mode, the input spectrum is channelized, up-sampled by a factor of 2, and down-sampled by 5-to-1 and 15-to-1 for output rates of 12 MHz and 4 MHz, respectively. Because of up-sampling by a factor of 2, there are 10 polyphase filter coefficient stages each with 6 taps. The filters' coefficients are periodically rotated through the 5 input registers (which have a periodic sliding input commutator) according to the state machine described in Table 4 and

▼ Table 5. Register loading sequence and the corresponding subfilter coefficients for 15/2 sample rate change in a 5-path polyphase filter

State	No of Inputs	Loading Sequence	Filter Coefficients
0	8	R4 R2 R0 R3 R1 R4 R2 R0	C0 C6 C2 C8 C4
1	7	R3 R1 R4 R2 R0 R3 R1	C5 C1 C7 C3 C9



▲ Figure 5. (a) Input signal spectrum with 5 channels of 3 MHz bandwidth and 6 MHz channel spacing at 30 MHz sample rate. The spectra of the 5 output channels are (b) 6 MHz for 5-to-1 down-sampling, (c) 10 MHz for 3-to-1 down-sampling, (d) 5 MHz for 6-to-1 down-sampling, (e) 12 MHz for 5/2 resampling, and (f) 4 MHz for 15/2 resampling.

Table 5. The spectral locations of the channels are reordered as a result of processing the up-sampled data in the polyphase filter [3], [5]. The 5-point FFT processes the polyphase data output frequencies in the order [0, 2, 4, 1, 3], which is seen to be indexing stride of 2 mod 5. These are reordered back to their natural order. Figs. 5(e) and (f) show the spectra of the 5 output channels at 12 MHz and 4 MHz, which correspond to 5/2 and 15/2 sample rate changes, respectively.

The simulations show that embedded sample rate changes can be successfully implemented in a polyphase channelizer. All the output channels have 60 dB of spectral side-lobe attenuation, selected by the prototype low-pass filter. The processing engines used in all the 5 cases are identical except that each has different state machines, register loading schemes, and subfilter coefficient sets.

5 Conclusion

In this paper, we have shown the versatility of a polyphase engine that

performs embedded resampling that is uncoupled from frequency selection and bandwidth control. Five embedded resampling modes in polyphase filter banks have been presented, namely, maximally decimated, under-decimated, over-decimated, and combined up- and down-sampling. These correspond to single, short, long, and multiple commutator stride lengths. For various applications, these modes can be used for any required rational sampling-rate change in an SDR front-end using a polyphase channelizer. The suggested modes are highly useful for designing flexible and resource-optimal architectures for advanced software radios. In a subsequent paper “Hardware Architecture Analysis of Polyphase Filter Banks Performing Embedded Resampling for Software Defined Radio Front-Ends” [6], we analyze FPGA based hardware architecture of these resampling engines in terms of area, time, and power tradeoffs.

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Design of Software-Defined Down-Conversion and Up-Conversion: An Overview

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Abstract: In recent years, much attention has been paid to software-defined radio (SDR) technologies for multimode wireless systems. SDR can be defined as a radio communication system that uses software to modulate and demodulate radio signals. This article describes concepts, theory, and design principles for SDR down-conversion and up-conversion. Design issues in SDR down-conversion are discussed, and two different architectures, super-heterodyne and direct-conversion, are proposed. Design issues in SDR up-conversion are also discussed, and trade-offs in the design of filters, mixers, NCO, DAC, and signal processing are highlighted.

Keywords: SDR down-conversion; up-conversion; direct-conversion; super-heterodyne conversion

1 Introduction

Software-defined radio (SDR) will play a key role in future radio configurations because of the emergence of new wireless technologies and their integration into fourth generation standards such as LTE-Advanced. SDR is a fundamental part of many radio systems, which include up-conversion of the discrete baseband signal into a high-resolution radio signal at the transmitter and down-conversion of the high-resolution radio signal back into baseband at the receiver [1]. Fig. 1 shows an SDR receiver in super-heterodyne architecture — a dual-stage conversion architecture in which a radio frequency (RF) signal is down-converted to intermediate frequency (IF) in the first stage and then converted from IF to baseband in the second stage. The hardware in the RF, IF, and baseband sections are controllable and reconfigurable using

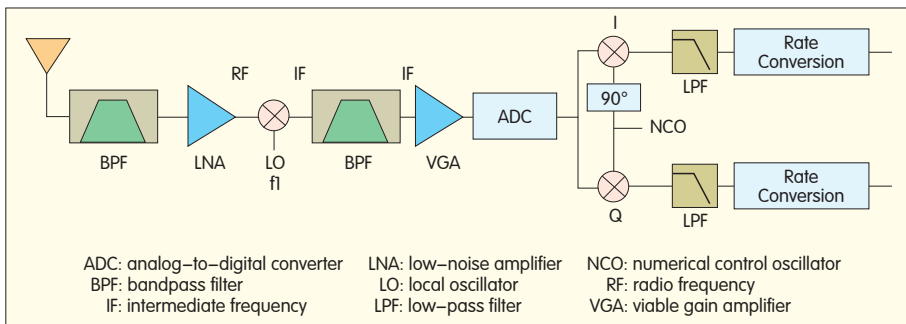
software (Fig. 1).

In Fig. 1, the RF front-end (analog front-end) is the only analog section and includes mixer, low-noise amplifier (LNA), power amplifier (PA), RF combiner, bandpass filter (anti-aliasing), and antenna. The RF front-end is responsible for transmitting and receiving RF signals and converting RF signals to IF. Some advanced RF front-ends allow a certain degree of control, for example, frequency tuning, through software.

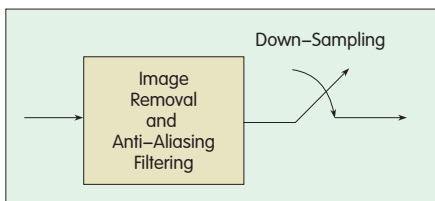
The other parts of the SDR architecture are digital processing components. In the IF section, sampling and separation of IF carriers, and up/down frequency conversion to baseband is performed by digital IF processing normally implemented in field programmable gate array (FPGA). Take the receiving path for example. The IF signal is digitized by the analog-to-digital converter (ADC) and then converted to baseband by digital IF processing. Digital IF processing

includes digital down-conversion (DDC) operations such as digital synthesizing, digital numerical control oscillator (NCO), digital mixing, I/Q demodulation, and multirate decimation filtering. In digital IF processing, digital up-conversion (DUC) is performed in the reverse order of DDC. Digital systems such as FPGAs are normally used for IF-to-baseband conversion because they are able to handle tight real-time constraints imposed by high-speed sampling and digital conversion. In the back-end of the SDR architecture, the baseband process mainly performs digital communications functions such as symbol timing recovery, equalization, modulation, and channel coding. These functions are usually carried out using digital signal processors (DSPs) with slightly relaxed real-time constraints.

SDR architecture tends to use general-purpose digital systems. FPGAs and DSPs in SDR allow the transmitted signal to be generated and



▲ Figure 1. Super-heterodyne receiver architecture.



▲ Figure 2. Sample rate conversion module in DDC with integral rate conversion.

the received radio signal (at the receiver) to be tuned and detected digitally by software. The conventional method involves an analog signal passing through individual hardware components, each of which perform a specific function. SDR systems offer greatly extended programmability, reconfigurability, and definability. SDR is intended to be a radio system that is flexible, versatile, and multistandard. This system is therefore able to accommodate updates of new radio functions.

This article highlights several possible implementations of receivers and transmitters. Several architectures for SDR receiver front-ends are reviewed alongside several architectures for transmitter front-ends. In the conclusion, we summarize this work and identify solutions with greatest potential from our point of view.

2 Software-Defined Radio Receiver Architectures

In this section, we review several front-end architectures for SDR receivers.

2.1 Super-Heterodyne Receiver

Fig. 1 shows a super-heterodyne receiver. Super-heterodyne is a

well-known receiver architecture in which an RF signal received from the antenna is translated to baseband using a down-conversion mixer, bandpass filter, and amplifier [2]. First, the signal is filtered by a bandpass filter (BPF) to obtain the desired channel signal. After BPF, the signal level is boosted by an LNA. The signal is converted to IF because of the down-conversion mixer, local oscillator (LO), second-stage BPF, and variable-gain amplifier. Then, it is sampled by an ADC and digitally processed by the DDC. At the DDC, I/Q components are extracted and demodulated to baseband. Because of the sample rate difference at IF and baseband, multirate filters are required to perform sample-rate conversion.

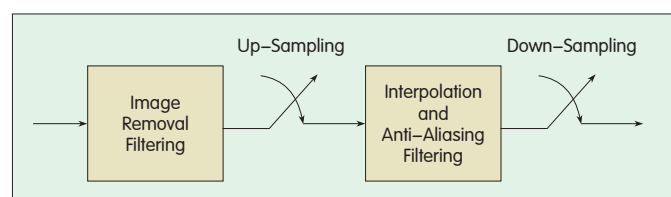
If the conversion rate is an integer, the sample-rate conversion module in the DDC performs image-removal filtering, anti-aliasing filtering, and down-sampling. This module can be jointly designed by using multistage or single-stage filtering. Such a design provides an equivalent impulse response for performing image-removal filtering and anti-aliasing filtering. The single-stage implementation is shown in Fig. 2.

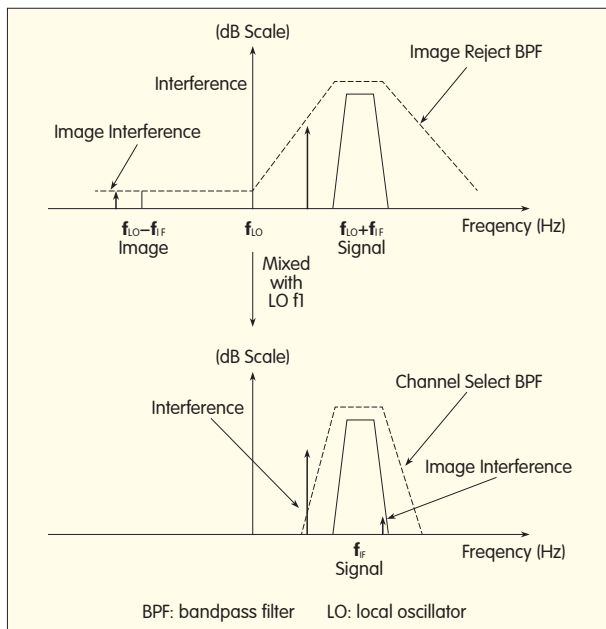
If the conversion rate is a fraction, the DDC module performs image-removal filtering, up-sampling, interpolation/anti-aliasing filtering, and down-sampling [3]. The filtering

operation cannot be jointly designed in this case. Fig. 3 shows the single-stage implementation of each filtering operation.

Currently, super-heterodyne architecture is used for higher-RF frequency designs such as LTE and IEEE 802.11ac. The main issue for super-heterodyne receivers is the high-quality image and adjacent filter design. Fig. 4 (top) shows the process of converting an RF signal into an IF signal. The received signal contains the desired signal at $f_{LO} + f_{IF}$, a second signal close to the image frequency at $f_{LO} - f_{IF}$, and interference in an adjacent channel [4]. The image signal is removed by an image-reject BPF before conversion. At this stage, adjacent interference and image interference cannot be completely removed because of the limitation of the image-reject BPF. The interference level is attenuated by the image-reject BPF. Fig. 5 shows that the remaining signal and interference at the image frequency falls into the same band as the desired signal when down-converted into IF. This down-conversion is performed by the mixer and the first LO. However, the image signal, while strongly attenuated by the image-reject BPF, is still present in the signal band at IF. The channel-select BPF cannot remove this interference. The higher the IF that is chosen, the better the image that can be rejected by a filter because the separation between the desired signal and image is greater. A considerable drawback of using a high IF is that signals in adjacent channels are not sufficiently attenuated by the image-reject filter and a subsequent IF filter becomes necessary. The lower the IF, the steeper the absolute slope of the filter. As a compromise, two different IFs can be used, which creates a dual-IF topology. A further drawback of the super-heterodyne receiver is its

Figure 3. Sample rate conversion module in DDC with fractional rate conversion.





◀ Figure 4. Spectrum conversion in a super-heterodyne receiver.

complexity, which leads to increased chip size, more complex circuit design, and increased power consumption in the direct-conversion receiver.

2.2 Direct-Conversion Receiver

Another approach for front-end architecture is the direct-conversion receiver as shown in Fig. 5. A direct-conversion receiver is a simplified version of a super-heterodyne receiver [5], [6].

The received RF signal is selected by a BPF and amplified by an LNA. The BPF removes out-of-band interference and noise. After this, the selected RF signal is directly down-converted to DC by a mixer and converted to digital by ADC. Only low-pass filters are needed in the baseband circuits to perform channel filtering. Compared with a super-heterodyne receiver, a direct-conversion receiver has fewer analog components. The absence of a high-Q filter is a significant advantage of a direct-conversion receiver, as is the completely integrated CMOS implementation of the front-end without the signal quality being impaired. Therefore, the direct-conversion receiver can make use of the high level of integration for multiband receivers. Issues for the direct-conversion receiver include DC offsets, even-order distortion, carrier leakage,

and I/Q imbalance [7], and each component has to be carefully designed and tuned. DC offset is generated by self-mixing a strong signal at the mixer stage. The strong signal is normally from interference or the LO signal. The down-conversion stage involves down-converting directly to zero frequency. A DC offset is amplified in baseband together with the received and down-converted signal. If the offset has higher amplitude than the desired signal, the offset dominates and saturates the following LNA [8]. In the even-order distortion, spurious signals are created at low frequencies because of the direct-conversion architecture. Because of RF to IF leakage in the mixer, products of even-order distortion in the LNA and mixer can damage the baseband signal. To

resolve this problem, differential circuits can be used for LNA and mixer, and the design of these circuits should be optimized for linearity. Leakage of the LO signal from the mixer and LNA creates in-band interference for other receivers. To resolve this problem, balanced mixers and LNAs with high reverse isolation are used in the design. In I/Q imbalance, the LO outputs are not exactly 90 degrees out of phase between the I and Q branches. This phase shift causes I/Q mismatch in the baseband. However, this distortion is frequency-independent, and digital calibration can remove it.

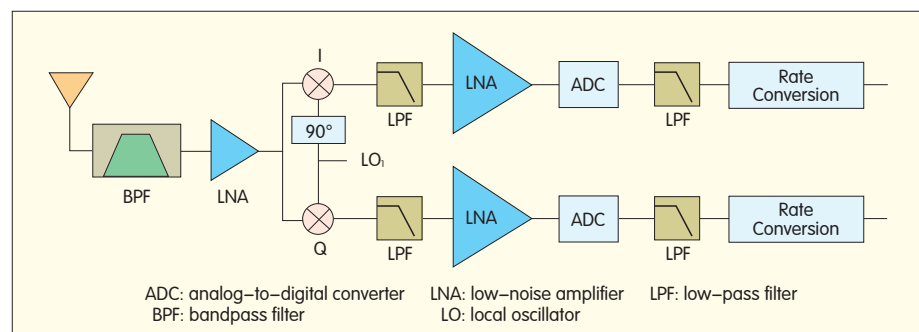
3 Software-Defined Radio Transmitter Architectures

3.1 Super-Heterodyne Transmitter

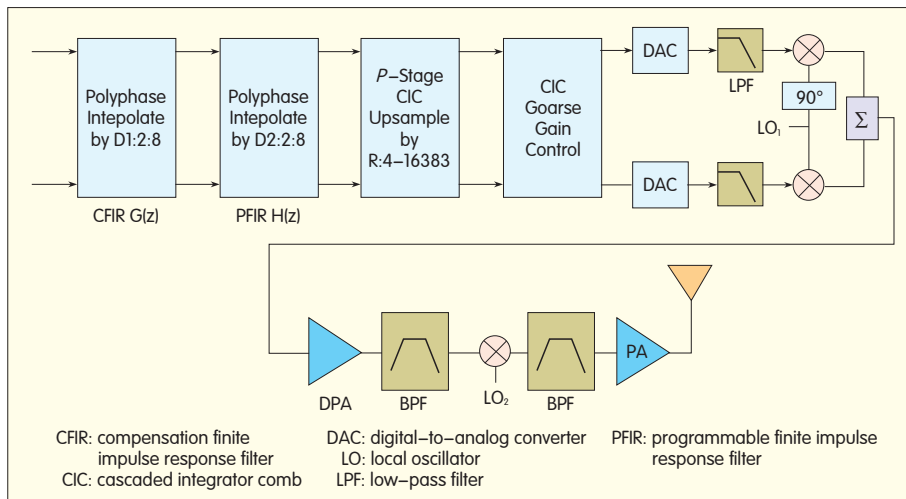
A super-heterodyne transmitter uses the reverse procedure of the super-heterodyne receiver shown in Fig. 6. The signal is created in the digital domain and then converted into analog using simple digital-to-analog converters (DACs).

The complex input I/Q baseband signal is sampled at a relatively low rate, typically the digital modulation symbol rate. The baseband signal is filtered and converted to a higher sampling rate before being converted into analog. Starting at the interpolation filter, the complex input signals pass through three stages of filtering, each of which changes the sampling rate and performs associated low-pass interpolation filtering [9]–[11].

The three filtering stages are shown in Fig. 6. First, a compensation finite impulse response filter, CFIR $G(z)$,



▲ Figure 5. Direct-conversion receiver architecture.



▲ Figure 6. Super-heterodyne conversion transmitter architecture.

provides a sampling rate that is increased (in step 2) from 1 to 8. The filter also performs Nyquist pulse shaping for the transmitter. Second, a programmable FIR filter, PFIR $H(z)$, increases the sampling rate by 2 and compensates for the passband distortion created by the third-stage cascaded integrator comb (CIC) filter. $G(z)$ and $H(z)$ are implemented with efficient multiplier-accumulator (MAC) blocks. Third, the P -stage CIC interpolation filter increases the sampling rate from 4 to 1448. The design parameters of the CIC allow for the synthesis of a circuit that has fixed sampling-rate increases or one where sampling-rate increases are programmable in real-time. Fourth, the CIC coarse-gain control block is needed to control the power distortion caused by CIC filtering. Finally, the complex data stream from the filtering stages is converted into an analog I/Q signal. In the analog domain (after DACs), the signal is modulated at an IF and is amplified and filtered to eliminate harmonics generated during modulation. The signal is then up-converted into RF by the second LO. This RF signal is filtered by another BPF to remove the image signal and is boosted by an RF PA [12].

A super-heterodyne transmitter architecture has two advantages. The I/Q modulator works at IF band, which means the circuit is much easier to design than at RF band. Also, the

overall signal level can be controlled at IF band. Therefore, it is much easier to design a high-quality variable-gain amplifier at IF band. However, such an amplifier has the same high complexity as the super-heterodyne receiver. Super-heterodyne transmitter architecture is therefore mostly used for wireless measurement instruments or backhaul wireless communication.

3.2 Direct-Conversion Transmitter

A direct-conversion transmitter has a simplified version of the super-heterodyne transmitter architecture [13] (Fig. 7). The design of the digital domain has exactly the same architecture as the super-heterodyne transmitter. The two DACs convert the digital signal into analog. The following

LPF removes the Nyquist images and improves the noise floor. Then, the complex analog I/Q signals are directly modulated at RF band by the high-specification RF I/Q modulator [14]. A BPF centered at the desired output frequency then removes the image signals. A final PA can boost the desired signal to a certain power level.

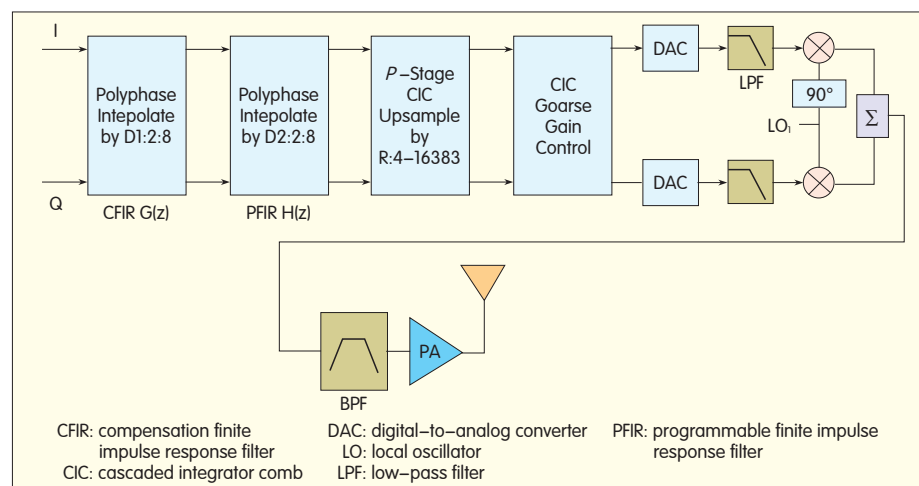
The most significant advantages of the direct-conversion transmitter are its versatility, flexibility, spectral efficiency, and low complexity. These make the transmitter simpler than the super-heterodyne transmitter. Small chip and circuit size and low power consumption can be achieved with a direct-conversion transmitter architecture.

Direct-conversion transmitter architecture is mostly used in multimode communication systems. By duplicating the hardware for each channel and each standard, a multimode radio DUC can be implemented.

Although direct-conversion architecture reduces the complexity of the transmitter design, it has some serious drawbacks, including carrier leakage and phase gain mismatch. Gain may need to be controlled at RF. The architecture also requires a PA with good linearity [15].

4 Conclusion

In this article, we have reviewed receivers and transmitters used in SDR



▲ Figure 7. Direct-conversion transmitter architecture.

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front-ends. Advantages and disadvantages of each design have also been analyzed. A well-designed architecture for multiband multimode receivers and transmitters should allow hardware resources to be optimally shared. The architecture should make use of software-controlled components and software-programmable devices. A direct-conversion approach was used in the transmitter and receiver front-end for implementation in most commercial wireless systems. Direct-conversion is the most appropriate architecture because it is low cost, consumes little power, and has a high-data-rate radio interface. However, system designers need to pay more attention to I/Q imbalance, carrier leakage, and DC offset in a direct-conversion receiver and transmitter system.

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Biographies

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Qing Xuan (jasx@talk2-1.com) received her Ph.D. degree in power and energy from the University of Bath in 1995. She has more than 20 years' experience in the telecom, energy, finance, and aviation sectors. Since March 2009, she has co-founded two companies. From January 2005 to March 2009 she was a business strategy director for Huawei Technologies. Her responsibilities included working with the minister and regulator to develop markets and introduce investor partners to clients. She also provided supply chain consultancy services to secured—business clients, including M&A Technology Company. From 2000 to 2004, Dr. Qing Xuan was a commercial and technical architect at Vodafone Group. From 1998 to 2000, she was as design engineer for Panasonic. From 1995 to 1998, she was post-doctoral researcher in the Power Group at the University of Bath. From 1987 to 1991, she was deputy director of the Telecom Department at the Ministry of Power and Water, China.

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Mikko Valkama is full professor and department head of the Department of Communications Engineering at Tampere University of Technology (TUT), Finland. He has been involved in organizing conferences such as the IEEE SPAWC'07 in Helsinki. He was awarded Best Ph.D. Thesis by the Finnish Academy of Science and Letters. His research interests include communications signal processing, estimation and detection techniques, signal processing algorithms for software defined flexible radios, and signal processing for cognitive radio. He is also interested in digital transmission techniques, such as different variants of multicarrier modulation methods and OFDM, and radio resource management for ad-hoc and mobile networks.

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Practical Non-Uniform Channelization for Multistandard Base Stations

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Abstract: A Multistandard software-defined radio base station must perform non-uniform channelization of multiplexed frequency bands. Non-uniform channelization accounts for a significant portion of the digital signal processing workload in the base station receiver and can be difficult to realize in a physical implementation. In non-uniform channelization methods based on generalized DFT filter banks, large prototype filter orders are a significant issue for implementation. In this paper, a multistage filter design is applied to two different non-uniform generalized DFT-based channelizers in order to reduce their filter orders. To evaluate the approach, a TETRA and TEDS base station is used. Experimental results show that the new multistage design reduces both the number of coefficients and operations and leads to a more feasible design and practical physical implementation.

Keywords: SDR; non-uniform; channelization; base station; TETRA

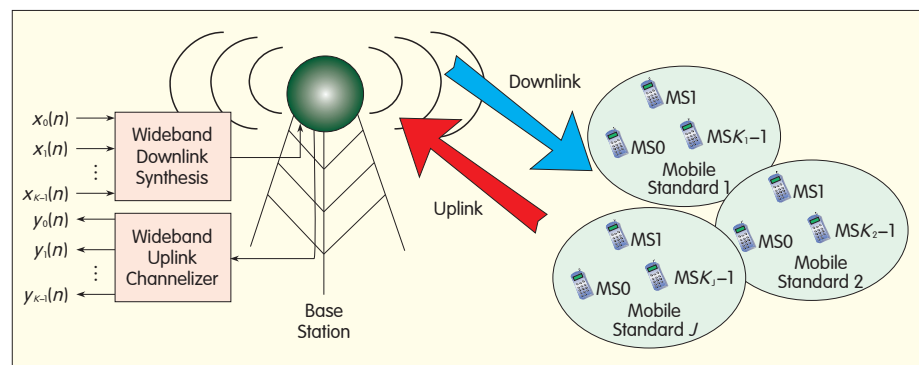
1 Introduction

Radio spectrum is typically allocated using coarse-grained frequency division multiplexing. Different radio standards are allocated independent and non-overlapping frequency bands that are reserved exclusively for each standard. This approach simplifies the radio design because each standard operates in isolation; however, available spectrum is not used optimally because reserved bands may be under-used some of the time. A more efficient alternative is to allow multistandard multiplexing of the frequency band. The frequency band is instead multiplexed among multiple radio standards [1]. Channels within the frequency band are dynamically allocated to the radio standards. If these channels do not have uniform bandwidth or center frequencies, as is typical for heterogeneous radio standards, then dynamic allocation is challenging.

In software-defined radio (SDR), analogue-to-digital and digital-to-analogue conversion is performed as close as possible to the antenna [2]. Most of the radio components, now in the digital domain, are implemented on a reconfigurable platform. Reconfigurability makes SDR particularly suitable for working with multistandard systems and for

upgrading to future standards.

In an SDR base station (Fig. 1), the wideband uplink, which comprises all the mobile station channels, is digitally converted immediately after the RF front-end. Multirate digital signal processing (DSP) is then used to filter and shift to baseband all the independent information channels. On the transmitter side, complementary



▲ Figure 1. Asymmetric system formed by SDR multistandard base station and single-carrier based mobile stations that use different mobile standards and uplink and downlink frequency bands.

processing is carried out. Extraction of the uplink channels (channelization) is a bigger challenge than downlink synthesis because more stringent filtering is required to avoid adjacent channel interference.

Different non-uniform channelization techniques have been described in [3]–[5]. In many cases, these techniques are based on combining or altering efficient uniform channelization methods, such as uniform complex discrete Fourier transform (DFT) modulated transmultiplexers and tree quadrature mirror filter banks (TQMFB) [6]. In these filter bank (FB) based structures, a synthesis bank multiplexes the channel frequency at the transmitter side, and an analysis bank performs for equivalent channelization in the receiver. Such a structure is symmetric; that is, amplitude and phase distortion in one half of the FB are suppressed in the complementary half, allowing perfect reconstruction. This approach includes multicarrier techniques such as OFDM. In contrast, the system in Fig. 1 has an asymmetric design; that is, the uplink signal channelized by the analysis bank is not created by a complementary synthesis bank. The system comprises the transmissions of independent mobile stations that are assumed to use single-carrier transceivers. The downlink is similarly asymmetrical. This structure allows the base station to be compatible with legacy systems. A professional mobile radio (PMR) base station using the terrestrial trunked radio (TETRA) standard or its high-speed derivative, TETRA enhanced data service (TEDS) [7], is a good application of this architecture.

In an asymmetric system, subcarriers and aliasing overlap because of down-sampling in the analysis bank. The overlap must be minimized by high-order filters [4], and these high orders are a bottleneck in the design and physical implementation of the channelizer filters. Multirate DSP techniques, such as multistage filtering, can significantly reduce the filter orders for more practical implementation. In this paper, we compare two non-uniform channelization

techniques, parallel generalized DFT–FB (GDFT–FB) and recombined GDFT–FB, by applying multistage filtering. We then evaluate these modified FBs in TETRA and TEDS base stations and compare their filter lengths and computational loads with those in [4]. Finally, the effect of multistage design on the physical implementation of the channelizer is considered.

Section 2 describes the non-uniform channelization requirements of a base station, specifically, TETRA and TEDS base stations and their possible updates. Section 3 describes the classic implementation of the two non-uniform channelization methods analyzed in this paper. Designs for methods to be used in TETRA and TEDS base stations are given. Section 4 describes a new multistage design for the two non-uniform channelization methods, and improvements in design and implementation are also described. Section 5 concludes the paper.

2 Frequency Multiplexed Spectrum for Next-Generation PMR

There are two main releases of TETRA: TETRA voice and data (V&D) and TEDS. The former supports 25 kHz channels that are mainly allocated in the 380–400 MHz frequency band. The latter was approved by the ETSI in 2005 and supports wideband services using 50, 100, and 150 kHz channels. However, the maximum throughput using TEDS is not enough for real-time applications. Therefore, the addition of a broadband communication system similar to one used in commercial 4G mobile communications is being investigated [8].

In a legacy base station, the antenna system can only cover 380–400 MHz, and adding extra antennas can be problematic because of electromagnetic restrictions in different countries [9]. As a result, a multistandard multiplexed frequency band has been proposed in which TETRA and TEDS channels share the 380–400 MHz band instead of occupying different bands. Prior to TEDS being released, countries

invested heavily in TETRA V&D networks, so it is important that any future updates are compatible with these legacy networks.

For all PMR standards, including TETRA and TEDS, the permitted channel centre frequencies, $f_c(n)$, are defined by

$$f_c(n) = \text{band_edge} + (n - \frac{1}{2}) \Delta f_c \quad (1)$$

where n is the channel number, band edge is the lower-edge frequency of the multiplexed frequency band, and Δf_c is the channel spacing [10]. The available spectrum is divided into frequency sub-bands that are equal to the channel spacing, and channels are centered within each sub-band.

In common hardware, the multiplexed frequency band solution requires fixed-channel allocation. Because the hardware cannot be easily reconfigured, different sections of the spectrum are allocated for different channel sizes. This solution has poor spectrum efficiency because the channel allocation is not optimized. The two SDR-based approaches described here allow reconfiguration so that channels can be dynamically allocated, and channels of different sizes can be adapted as required. This means that spectrum can be used more efficiently.

To test these non-uniform channelization structures, we created a scenario where the standard 380–400 MHz PMR band was shared by TETRA 25 kHz and TEDS 25, 50, and 100 kHz channels. In this band, the 5 MHz between 380–385 MHz was reserved for the uplink signal, and the 5 MHz between 390–395 MHz was used for the downlink signal. TEDS 150 kHz channels were not considered, but the procedure can be extended to 150 kHz channels.

3 Non-Uniform Channelization Based on GDFT–FB

Channelization methods can be uniform or non-uniform depending on their capacity to filter channels that have equal or different bandwidths within the same frequency band.

Uniform channelization using polyphase DFT-FBs has been proposed for real-world applications that have a large number of (uniform) channels. Various methods have also been proposed for non-uniform channelization [3], [5], [11]–[12]. However, methods based on uniform DFT-DB are particularly attractive because of its low implementation complexity.

Rather than using DFT-FB directly [6], GDFT-FB is used. GDFT-FB gives additional control over channel frequency allocation and phase response because it has two parameters in the subfilter complex modulation [13]. In the filter bank, k filters are obtained by complex modulation of the lowpass prototype filter, $H(z)$:

$$H_k(z) = W_K^{-(k+k_0)n_0} H(zW_K^{(k+k_0)}) \quad (2)$$

where $W_K = \exp(j2\pi/K)$, and K is the number of sub-bands of the analysis bank. The parameter k_0 determines the way different sub-bands are stacked on the spectrum, and n_0 determines the phases of the different channels. If $k_0 = 0$ and $n_0 = 0$, the sub-band spectrum allocation is even-stacked, and the first sub-band is centred at DC. In this case, the GDFT-FB structure is reduced to the classic DFT-FB. If $k_0 = 1/2$ and $n_0 = 0$, the spectrum allocation is odd-stacked; that is, the sub-bands are shifted half the channel spacing, and no channel is centred at DC. An odd-stacked approach is used in the proposed non-uniform designs because it meets the channel allocation restrictions defined by (1). Different values of n_0 can be chosen to provide extra phase shifts to the FB outputs. In the even- and odd-stacked cases, the sub-band spacing is

$$\Delta f = f_s/K \quad (3)$$

where f_s is the sampling frequency of the wideband multichannel analysis bank input signal.

The prototype filter, $H(z)$, may be decomposed into its polyphase components according to

$$H(z) = \sum_{i=0}^{K-1} z^{-i} E_i(z^K) \quad (4)$$

where E_i are the polyphase components [6]. The rest of the sub-filters, $H_k(z)$, expressed in (2) can then be obtained from

$$H_k(z) = W_K^{-(k+k_0)n_0} \sum_{i=0}^{K-1} z^{-i} W_K^{-ki} W_K^{-k_0} E_i(z^K \cdot W_K^{-k_0}). \quad (5)$$

The general implementation of the analysis GDFT-FB for even- and odd-stacking cases is shown in Fig. 2. From (5), the different complex exponentials are applied to the different branches in order to obtain the desired sub-band stacking and phase shifts. The complex exponentials, $W_K^{-k_0}$ and W_K^{-ki} , can be directly hard-coded into the polyphase components of the filter bank, and W_K^{-ki} denotes the DFT algorithm. After the DFT, $W_K^{-k_0 n D}$ is applied in order to present the different outputs, $y_k(n)$, centred at DC. Finally, $W_K^{-(k+k_0)n_0}$ is applied to the outputs for phase shift purposes. Depending on the values of the decimation factor, D , the filter bank can be critically sampled ($K=D$) or oversampled ($K=LD$), where L denotes the oversampling factor. The main benefit of an oversampled FB is that aliasing due to decimation is significantly reduced [14]. However, an oversampled FB has additional computational load because it runs at a higher sample rate (by a factor of L).

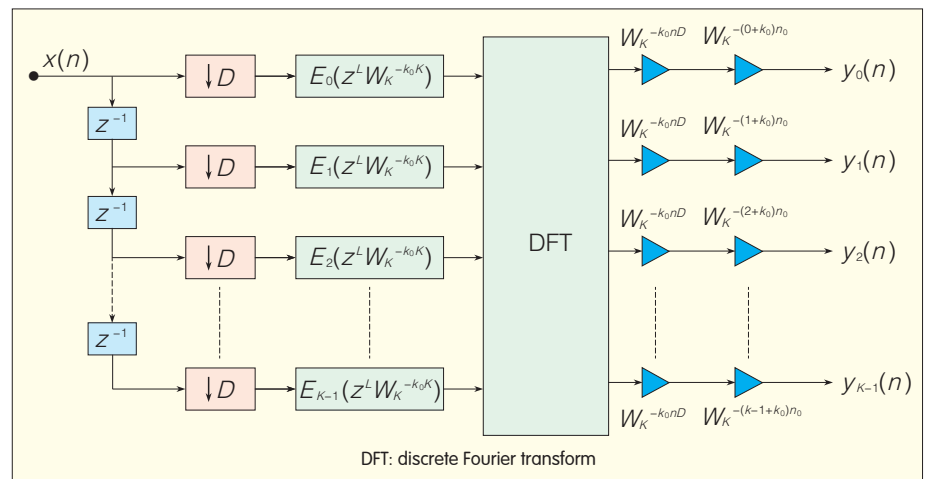
3.1 Parallel GDFT-FB

A parallel GDFT-FB is proposed in [4], [15] as a non-uniform channelization solution for base stations. The wideband signal is

processed through different critically decimated odd-stacked GDFT-FBs operating in parallel. Each FB uniformly divides the frequency band according to specific channel spacing, and the FBs have overlapping frequency. In [15], the transmitter (synthesis) side is described, and in [4], the receiver (analysis) side is described.

In the parallel GDFT-FB channelizer, the digitized wideband signal with sample rate f_s , is fed into multiple filter banks running in parallel. There is one filter bank for each uniform channel frequency plan. Narrowband channels are extracted by selecting an appropriate subset of outputs from each filter bank. Any permissible combination of channels can be specified by choosing the appropriate filter banks and channel numbers. Changing channel allocation in real-time does not require redesign or re-optimization of the filter bank structure. Only selection of appropriate outputs needs to be adapted.

Fig. 3 shows the parallel GDFT-FB for the 5 MHz uplink band of a TETRA/TEDS base station. In this band, there are 200 channels for TETRA V&D and TEDS 25 kHz. For TEDS 50 kHz, there are 100 channels, and for TEDS 100 kHz, there are 50 channels. DFT modulation is implemented using a power-of-2 FFT for efficiency; thus, the filter bank sub-bands cover a bandwidth larger than the frequency band containing the information channels. The excess sub-bands



▲ Figure 2. Generalized DFT analysis filter bank structure.

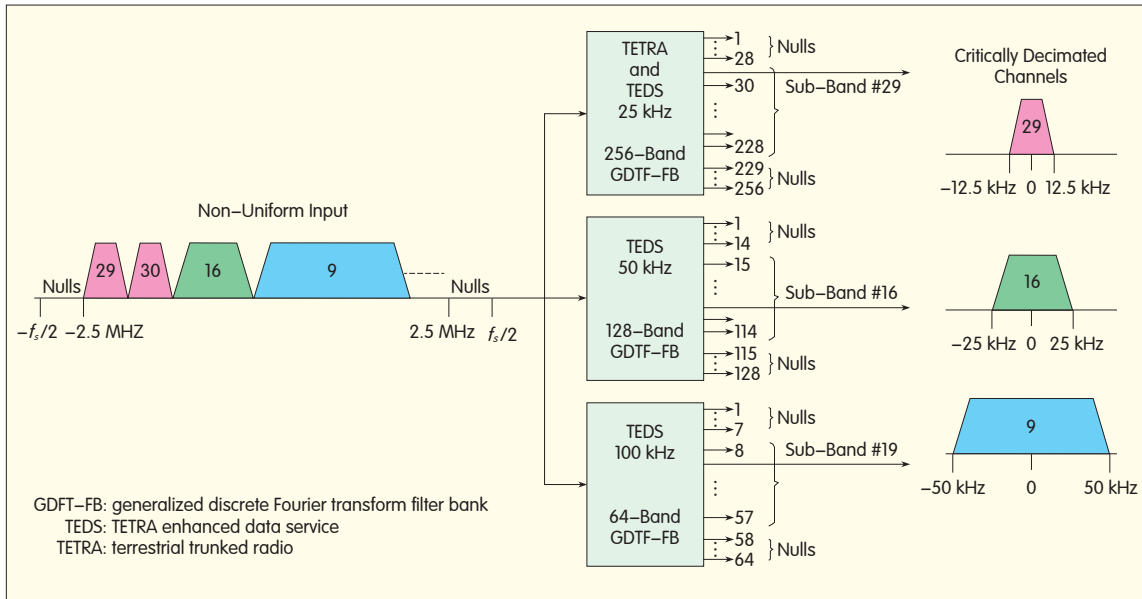


Figure 3. Parallel GDFT-FB channelization structure.

outside the 5 MHz bands are permanently null.

For the input signal in Fig. 3, starting from the lower edge (−2.5 MHz), the first two TETRA/TEDS 25 kHz channels are extracted from branches 29 and 30, respectively, of the first (25 kHz) FB. The next channel in the multiplexed spectrum, a 50 kHz TEDS channel, is selected as branch 16 of the second (50 kHz) FB. Branch 15 refers to the same frequency range as branches 29 and 30 of the 25 kHz FB. Similarly, the next channel in the multiplexed spectrum, a TEDS 100 kHz channel, is selected as branch 9 of the third (100 kHz) FB.

In the parallel GDFT-FB, the design can be critically decimated or oversampled. The critically decimated design has more aliasing from adjacent bands, whereas an oversampled design has a higher computational load. The level of aliasing interference that can be tolerated depends on the radio standard specifications.

Parallel configuration is not the best solution when the channel spectrum is not allocated according to (1), that is, when the possible channel center frequencies are not constrained to be a multiple of the channel spacing. In this case, additional GDFT-FBs must be added to the parallel structure so that each center frequency can be covered by at least one GDFT-FB. Even with

some constraints, the recombined GDFT-FB structure is a more flexible non-uniform channelization method.

3.2 Recombined GDFT-FB

A non-uniform recombination FB first divides a signal into uniformly spaced sub-bands and then recombines certain groups of sub-bands to form wider bandwidths that are an integer multiple of the uniform spacing (Fig. 4a). The sub-band bandwidth is the granularity band, and chosen according to the application requirements.

Non-uniform, recombined FBs have been proposed in literature on audio and speech processing [16]. In these applications, the FBs are critically decimated, so a perfect reconstruction algorithm with parameter optimization is needed to cancel the resulting aliasing. However, because of the asymmetric configuration shown in Fig. 1, such an algorithm is not possible.

Oversampling ensures that aliasing in the transition bands of the sub-band bandpass filters is less than that in the critically sampled case. Non-uniform channelization using recombined, oversampled FBs has been proposed in [4], [17], [18]. Recombination is carried out by the structure shown in Fig. 4(b). A recombined signal, denoted $Y_{k,R}(z)$, is formed by R contiguous sub-bands allocated from the k th

output of the GDFT-FB onwards:

$$Y_{k,R}(z) = \sum_{r=0}^{R-1} e^{j\varphi_r} Y_{k+r}(z^M) H_M(z e^{-j\beta_r}). \quad (6)$$

Therefore, channels are recombined by interpolating each of the R sub-bands by a factor M , frequency shifting by β_r to the correct center frequency, and phase correcting by φ_r in order to combine these shifted in-phase channels. To minimize amplitude distortion in the recombined channels, an amplitude-complementary prototype filter is required [19].

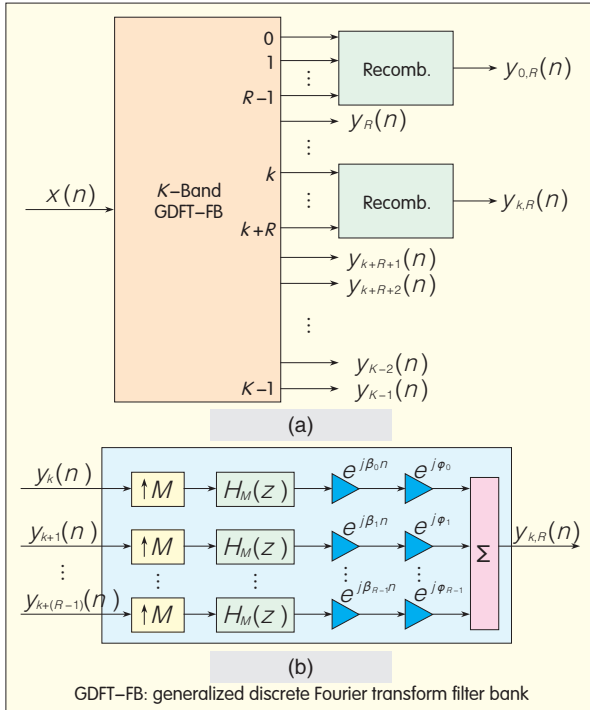
Because the GDFT-FB outputs are already oversampled by a factor L , the interpolation factor can be $M=R/L$. Hence, the frequency and phase shifts are, respectively,

$$\beta_r = \pi + \frac{\pi}{R}(2r+1) \quad \text{for } r = 0, \dots, R-1 \quad (7)$$

$$\varphi_r = -\left(\frac{MN}{2D} + \frac{N_M}{2D}\right) \beta_r \quad \text{for } r = 0, \dots, R-1 \quad (8)$$

where N_M is the order of the interpolation filter, and N is the order of the GDFT-FB prototype filter. To improve the structure in Fig. 4(b), the phase shift, φ_r , can occur before the interpolation. This means the phase shift is carried out at a lower sample rate than the anti-image filtering and frequency shift.

The FB is designed to cover an uplink frequency band of 5 MHz and deliver



▲ Figure 4. Recombined GDFT-FB channelizer (a) structure, (b) detail on the recombination structure.

narrowband outputs with bandwidth and channel spacing of 25 kHz. However, the sample rate of the narrowband channels is twice the channel spacing, that is, $K = 2D$, because of oversampling. In this particular case, the bandwidths covered are multiples of each other, and the chosen granularity band is 25 kHz. Consequently, the TETRA/TEDS 25 kHz channels may be selected directly, without any recombination, from the appropriate output sub-bands of the GDFT-FB.

For the wider 50 kHz and 100 kHz channels, adjacent output sub-bands of the FB must be recombined using the structure in Fig. 4. TEDS 50 kHz channels are obtained by recombining two outputs. The channels do not require additional interpolation prior to frequency shifting and combining because of the original oversampling. A TEDS 100 kHz channel is obtained by interpolating each channel by 2 and then frequency shifting and combining.

3.3 Evaluation of Channelizers

The parallel GDFT-FB and recombined GDFT-FB have the same

fundamental channelization capabilities when applied to channels whose bandwidths are related by integer multiples of each other. In these circumstances, parallel GDFT-FB is best for schemes with few possible channel bandwidths and alignment patterns; for example, TETRA/TEDS only has 3 such bandwidth and alignment patterns. However, recombination is best for schemes with a greater variety of channel bandwidths and alignment patterns. By decreasing the granularity bandwidth of the recombined GDFT-FB sub-bands, a wider range of recombined bandwidths is possible. Also, a wider range of center frequencies is possible for applications that do not necessarily

conform to (1).

Channelization structures dynamically filter channels with different bandwidths; however, these structures can be differentiated according to computational load, filter design complexity, and filter implementation complexity.

For complex I and Q input samples, the number of real multiplications and additions for each complex input sample in an analysis or synthesis odd-stacked GDFT-FB are, respectively,

$$\mu_{\text{GDFT}} = \frac{L}{K} [4(N+1) + 4(\frac{K}{2}(\log_2(K)-1)) + 4K] \quad (9)$$

$$\alpha_{\text{GDFT}} = \frac{L}{K} [4(N+1 - \frac{K}{2}) + 2(\frac{3K}{2}(\log_2(K)-1)) + 2K] \quad (10)$$

where the first term is the number of arithmetic operations for the N -order complex-valued prototype filter, the second term is the number of arithmetic operations due to the complex-valued K -point radix-2 FFT [20], and the last term is the number of arithmetic operations due to multiplication by a

complex exponential signal. If the GDFT-FB is oversampled, $L > 1$. The number of arithmetic operations due to the K -point FFT could be reduced by using more efficient FFT algorithms, such as the split-radix FFT algorithm. However, power-of-2 FFT algorithms, such as the radix-2 and radix-4, are preferred for practical implementation on FPGAs [21].

For the parallel GDFT-FB, the computational load is the sum of the computational loads of each component GDFT-FB. Because all the GDFT-FBs run in parallel all the time, the total computational load is constant regardless of the channel allocation pattern.

In comparison, the computational load of the recombined GDFT-FB comprises a fixed part that corresponds to the oversampled GDFT-FB structure and a variable part, whose complexity depends on the number of recombined channels. The additional number of real multiplications and additions per input sample in each recombination structure (Fig. 4) are given by (11) and (12), respectively:

$$\mu_{\text{RECOMB}} = \frac{L}{K} [M \times R (2\frac{N_i+1}{2} + 4 + \frac{4}{M})] \quad (11)$$

$$\alpha_{\text{RECOMB}} = \frac{L}{K} [M(R(2N_i + 2 + \frac{2}{M}) + 2(R-1))] \quad (12)$$

where R is the number of sub-bands to be recombined into a wider channel, M is the interpolation factor required for recombination, and N_i is the order of the anti-alias filter required in the interpolation. To make the evaluation more concrete, the TETRA and TEDS specifications are applied to both the parallel GDFT-FB and recombined GDFT-FB. The specifications require a stop-band rejection of 55 dB for sufficient channel selectivity. A passband ripple of 0.1 dB is selected to minimize the amplitude distortion. The length of the FIR prototype filters used in both channelization structures is calculated using [22], and the Parks-McClellan equiripple algorithm is used [23]. The asymmetric system design in Fig. 1 creates aliasing in the channels of the receiver analysis bank, which is minimized by tight filter

specifications. This aliasing is especially significant in the critically sampled case [14].

To approximate the order of the different filters, the following equation is used [24]:

$$N \approx \frac{-20\log_{10}(\sqrt{\delta_p\delta_s})-13}{14.6[(\omega_{\text{stop}}-\omega_{\text{pass}})/2\pi]} \quad (13)$$

The filter order is a function of the passband ripple, δ_p , stop-band attenuation, δ_s , and normalized transition bandwidth ($\omega_{\text{stop}} - \omega_{\text{pass}}$) where $\omega = 2\pi f/f_s$. Consequently, for the same values of δ_p , δ_s , f_{pass} , and f_{stop} , the sample frequency, f_s , determines the normalized transition band and filter order. For channelizers with a large number of channels, the sample frequency of the wideband signal is much larger than the normalized transition band, and this leads to very high orders.

When applied to the TETRA and TEDS standards, the 25 kHz prototype filter for both channelizer structures has an order of 8085 taps. For the parallel GDFT-FB, the required prototype filter orders for the 50 kHz and 100 kHz FBs are 3584 and 1444 taps, respectively. However, these filter orders are only theoretical; the actual filter orders may be higher [4] because interchannel interference and aliasing produced by decimation in the analysis bank causes the filters' frequency response to deteriorate [14]. As the number of channels increases, aliasing also increases, and additional filter overdesign is required.

Each GDFT-FB requires only one prototype filter design; however, in the case of TETRA/TEDS, the large filter orders make designing the filter and implementing the corresponding channelizer structures impractical. Large filter orders can be expected for other radio standards with similar specifications.

This impracticality arises because the efficient implementation of a filter in a reconfigurable hardware platform typically requires fixed-point representation of filter coefficients. Coefficients must be quantized to the word length of the device, and the resulting quantization error may change

the filter transfer function [25]. In an FIR filter, these changes can lead to deviations in the magnitude response (particularly the stop-band attenuation), and this renders the filter unsuitable for certain applications. The problem is greater with high-order filters because quantization errors affect the position of filter zeros in the z -domain, and the distance between zeros is reduced. Therefore, the frequency response of high-order filters is more sensitive to small changes in the zero positions than the frequency response of low-order filters.

4 Modified GDFT-FB for Filter Coefficient Reduction

Although the parallel GDFT-FB and recombined GDFT-FB are flexible and more efficient than other structures, high filter orders are still required for TETRA/TEDS. For high-order channelization structures and, more generally, in communication applications, FIR filters are chosen because of their linear phase response. To achieve a linear phase response in an FIR filter of length $N+1$, where N is the order, $(N+1)/2$ coefficients contribute to the magnitude response of the filter, and the other half of the coefficients provide the linear phase property [22]. As a consequence, an FIR filter design generally requires a larger number of coefficients compared with other designs. For applications where perfect linear phase response is not required, a minimum-phase FIR or infinite impulse response (IIR) filter can provide a functionally equivalent magnitude response with a reduced number of filter coefficients.

When linear phase response is required, multistage filtering [26] is a useful technique that can be applied to FIR filter design to reduce the total number of filter coefficients. Multistage filtering is most commonly applied to interpolators and decimators that have large sample rate conversion factors. In a multistage filter design, an original filter is factorized into multiple component filters which, when cascaded, produce the original filter magnitude and phase response.

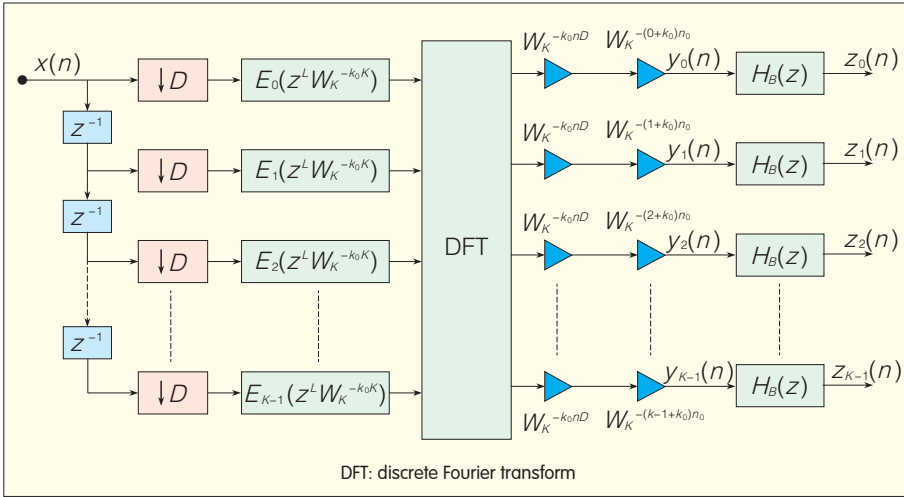
Component filters have more relaxed specifications than the original filter. Therefore, the number of coefficients in each component filter is smaller (often much smaller) than the original filter. The design of each component filter is also simplified, and the total computational load is often less than the original filter.

Here, we show that multistage filtering can be extended to modulated FBs and, in particular, to the GDFT-FB. In FB literature, the term multistage typically refers to a structure in which multiple FB stages are cascaded to form a complete FB [5], [27]. In the approach presented here, the multistage technique is applied to the prototype filter of only one FB.

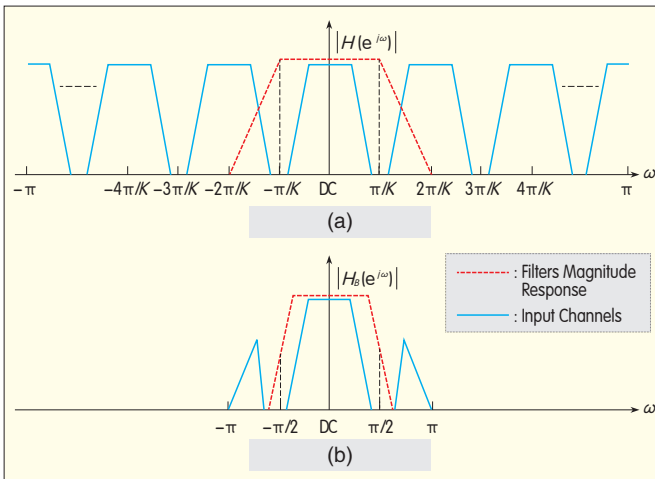
There are various ways in which the multistage technique could be applied to the prototype filter. The specification of the prototype filter, $H(z)$, and its polyphase components, is relaxed, and a half-band filter, $H_b(z)$, is applied to every sub-band output to obtain the original filtering specifications. This design is shown in Fig. 5.

In the single-stage design, the prototype filter transition band is narrow and centered at π/K . In the multistage design, the prototype filter transition band is shifted so that it starts at π/K and its width is increased so that it extends to $2\pi/K$ and includes frequency components from adjacent channels. The half-band filter on each sub-band output provides the original sharp transition band and also eliminates the undesired frequency components from the adjacent channels passed by the relaxed prototype filter. This filtering process is shown in Fig. 6.

For a multistage GDFT-FB, the FB cannot be critically decimated, but it has to be oversampled by 2, that is, $K = 2D$. Oversampling prevents the undesired adjacent-channel frequencies from aliasing with the channel of interest. Also, oversampling by 2 allows the use of half-band filters. This is attractive because half-band filters have desirable impulse and frequency response properties in Fig. 7(a). Half-band filters have a symmetric impulse response where



▲ Figure 5. Multistage analysis GDFT-FB. A half-band filter is added after every sub-band output.

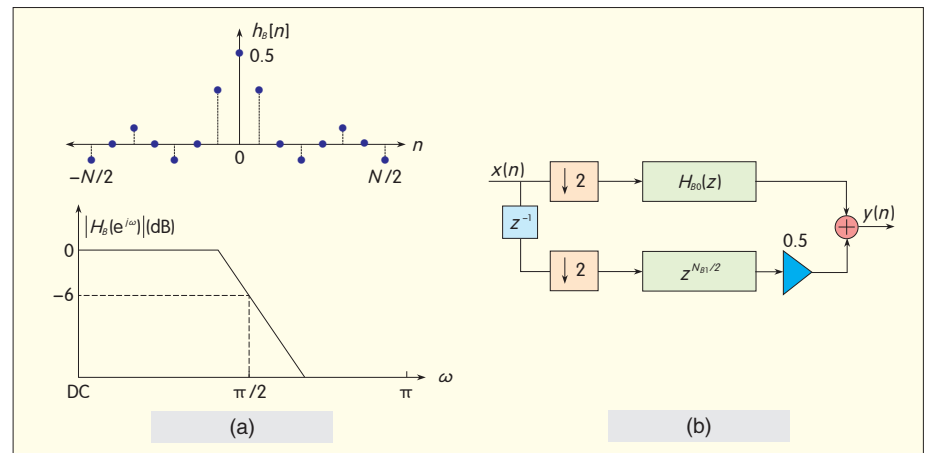


◀ Figure 6. multistage GDFT-FB filtering operations applied to one of the information channels. (a) GDFT-FB filtering of the channel centered at DC with relaxed transition band. (b) Half-band filter performing the sharp filtering of the channel and eliminating the frequency components from adjacent channels.

every second coefficient is zero; therefore, in implementation, only approximately 1/4 of the half-band filter coefficients have to be computed. In terms of frequency response, half-band filters allocate the -6 dB point at exactly $\pi/2$ radians. This makes them useful for recombined GDFT-FBs because the magnitude complementary property is easily achieved. Further advantages can be gained from the two-band polyphase implementation of the half-band filter using (4). This implementation allows down-sampling to be performed before the filtering. Also, because of the zero-value coefficients, one of the polyphase branches is formed by a pure delay and is followed by the middle filter coefficient [23]. Combined, these two advantages lead to fewer

operations per second than in the non-polyphase implementation.

By adding extra filter operations to (9)



▲ Figure 7. (a) Half-band filter impulse and frequency response (b) Efficient polyphase implementation of half-band filter plus decimator.

and (10), the number of real multiplications and additions per complex input for the channelizer is now determined by

$$\mu_{M-GDFT} = \frac{L}{K} [4(N+1) + 4(\frac{K}{2}(\log_2(K)-1)) + 4K + 2K \frac{(N_B+1)}{8}] \quad (14)$$

$$\alpha_{M-GDFT} = \frac{L}{K} [4(N+1) - \frac{K}{2} + 2(\frac{3K}{2}(\log_2(K)-1)) + 2K + 2K \frac{N_B}{4}] \quad (15)$$

where N_B is the order of the half-band filters.

This multistage GDFT-FB can replace the single-stage GDFT-FB in the parallel and recombined GDFT-FB channelization methods without any significant changes being made to these methods. For the recombined GDFT-FB, the phase shift introduced in the recombination structure shown in Fig. 4 and described by (7) is now changed to

$$\phi_r = -[M(\frac{N}{2D} + \frac{N_B}{2} + \frac{N_M}{2})]\beta_r, \quad \text{for } r = 0, \dots, R-1 \quad (16)$$

which compensates for the changed phase response slope introduced by the half-band filters on each sub-band output.

4.1 Channelizers Evaluation Using multistage GDFT-FB

To demonstrate the advantages of reducing the coefficients in the multistage design, the same TETRA/TEDS examples used for the

▼ Table 1. Filter orders calculated for TETRA/TEDS non-uniform channelizers using multistage GDFT-FB

	GDFT-FB Output Sub-Band Bandwidth (kHz)	Single-Stage Number of Coefficients	multistage Number of Coefficients
Parallel GDFT-FB	25	$N = 8085$	$N = 1294, N_s = 64$
	50	$N = 3584$	$N = 595, N_s = 58$
	100	$N = 1444$	$N = 291, N_s = 46$
Recombined GDFT-FB	25	$N = 8085$	$N = 1294, N_s = 64$
GDFT-FB: generalized discrete Fourier transform filter bank			

▼ Table 2. Number of coefficients and computational load of the TETRA/TEDS non-uniform multistage channelizers compared with single-stage design

	multistage Parallel GDFT-FB	multistage Recombined GDFT-FB
Percentage of Coefficients Compared with Single-Stage Design	16.7%	16.0%
Percentage of Real Multiplications Compared with Single-Stage Design	70.6%	35.3%
Percentage of Real Additions Compared with Single-Stage Design	92.3%	45.0%
GDFT-FB: generalized discrete Fourier transform filter bank		

two non-uniform channelization methods are used here. The theoretical filter orders are calculated again using (13). Even though the multistage design has two filters instead of one, it has two main advantages: its prototype filter is designed with a much larger transition band, and the half-band filter is designed for a much lower sample rate. Both factors contribute to reducing the filter orders shown in Table 1.

A reduction in the number of coefficients also implies a reduction in the number of operations per complex input sample (Table 2). For the multistage recombined GDFT-FB in Table 2, the figures represent only the GDFT-FB part of the channelizer. The structure used to recombine the TEDS 50 kHz and 100 kHz channels is the same for both single and multistage cases and is not included for that reason. The saving on multistage filtering computational load is greatest in the recombined GDFT-FB.

The performance of the two non-uniform channelizers can be compared in terms of their total number of real multiplications per sample for different sub-band allocation patterns [4]. Both architectures were tested in scenarios where the frequency band is covered with a single type of channel, for example, 25, 50, or 100 kHz, or where it is covered by various types of channels, for example, 50 and 100 kHz.

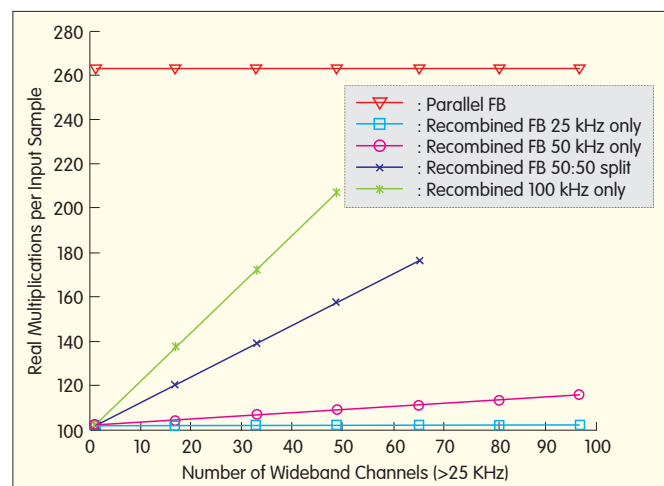
The test results are shown in Fig. 8. The parallel GDFT-FB has a constant computational load that is independent of the sub-band allocation pattern. On the other hand, the computational load of the recombined GDFT-FB varies according to the number and type of recombined channels. The load is at a minimum when the whole frequency band is covered by 25 kHz channels because no recombining is required. The load is at a maximum when the frequency band is fully occupied by TEDS 100 kHz channels; that is, recombination is applied to every GDFT-FB output sub-band. In contrast to the results obtained in [4], the recombined GDFT-FB using multistage filtering is more efficient than the

equivalent parallel GDFT-FB in every situation. The reason for this is that multistage filtering has a greater effect on the recombined GDFT-FB.

For the multistage channelizers, the filter orders were again obtained using theoretical calculations (section 3.3). However, real implementations require higher filter orders because of undesired effects, such as aliasing, in the FBs (Fig. 9). In Fig. 9, a channelizer for eight 25 kHz channels was designed using the single-stage and multistage GDFT-FBs. The theoretical order for the single-stage prototype filter was 253, whereas that for the multistage prototype filter was 42, and the half-band filter order was 64. All filters were designed as optimal equiripple filters.

Because of aliasing, the magnitude response does not exhibit 55 dB of attenuation in the stopband for the single-stage design. For the multistage design, the cascade of the two filters produces decay in the stopband that provides the desired attenuation in most of the stopband. In the passband, both filters provide a ripple within the 0.1 dB limits. To conform to the required specifications, an overdesign of the ideal prototype filter is needed to compensate for the aliasing. This usually leads to filter orders that are larger than the theoretical orders, especially in the single-stage design. Optimization techniques are outside the scope of this paper, but Kaiser-Window filters could possibly be used instead of optimal equiripple

Figure 8. ► Performance of parallel GDFT-FB and recombined GDFT-FB when multistage filtering is applied compared with [20].



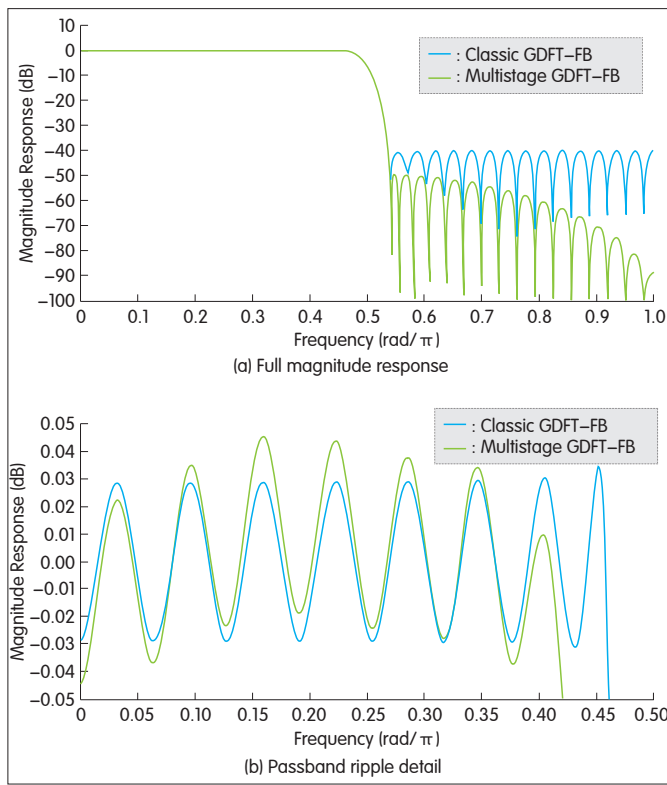


Figure 9. Classic and multistage GDFT-FB output magnitude response for an 8-channels TETRA channelizer.

ones. In normal circumstances, filters designed with the Kaiser-Window method need more coefficients than optimized filters. On the other hand, they have decay in their stopband that minimizes aliasing when applied to FBs [28].

4.2 Fixed-Point FPGA Channelizer Implementation

Physical implementation of parallel GDFT-FB and recombined GDFT-FB channelizers is aided by efficient FIR design and FFT processing tool boxes such as the Xilinx LogiCORE FIR Compiler [29] and Xilinx LogiCORE FFT [21] (which can be used with Virtex and Spartans FPGAs). These toolboxes support most of the component parts of the parallel GDFT-FB and recombined GDFT-FB structures. Nevertheless, such toolboxes often have limitations; for example, the FIR compiler limits filters to 1024 coefficients. With minor filter optimization, the multistage channelizers could be implemented with these toolboxes. However, the coefficient limitation prevents these toolboxes being used to implement single-stage channelizers because

they require much higher filter orders. Single-stage implementations might still be possible using a customized design, but this implementation requires longer development time.

Mobile communication systems generally use modulation schemes based on real-value in-phase and quadrature (I/Q) signals. For these modulation schemes, complex signal processing is useful for simplifying the signal operations and notation. Instead of considering the real-value I/Q input signals separately, in complex signal processing the I/Q signals are mapped on a complex input value as the real and imaginary parts respectively [30]. However, the system must be physically implemented using real signal operations. Consequently, the real-value I and Q components are processed in two different physical paths. Filtering or frequency mixing has to be applied to both components separately. For the filter implementations, depending on the desired odd or even sub-band stacking configuration of the GDFT-FB, the coefficients of the FB prototype are either real- or complex-valued, as

shown in (5). For real filters, the real-value coefficients of the prototype filter $H(z)$ are applied independently to the I and Q components (Fig. 10), where $R(z) = H(z)$ and $Q(z) = 0$. In contrast, complex digital filter implementations require more resources because their complex coefficients need to be reduced to real values [30]. For these implementations, the two real-value filter components, $R(z)$ and $Q(z)$, are obtained from the complex filter $H(z)$:

$$R(z) = \frac{H(z) + H^*(z)}{2} \quad (17)$$

$$jQ(z) = \frac{H(z) - H^*(z)}{2} \quad (18)$$

Like real FIR filters, complex FIR filters have symmetric properties that can be exploited in the $R(z)$ and $Q(z)$ implementation [31]. Therefore, a complex filter requires twice the number of multipliers as a real digital filter of the same length. The even-stacked GDFT-FB with real-value coefficients enables efficient physical implementation. Fixed-point representation is also important in physical implementation. For multirate filter banks, using fixed-point arithmetic to represent coefficients and signals produces errors such as analogue-to-digital input quantization noise, coefficient quantization errors, rounding errors, overflow errors, and sub-band quantization errors [32]–[33]. In FIR prototype filters, coefficient quantization errors do not affect the linear phase response characteristics but can affect the magnitude response. By using the multistage design with lower-order filters, the zeros in the z -plane are further apart; therefore, the filter magnitude response is less sensitive to quantization error than in filters with higher-order single-stage designs [25].

5 Conclusion

In this paper, we have described the practical implementation of two non-uniform channelization techniques based on GDFT-FBs. These FBs are efficient and flexible, but the use of FIR

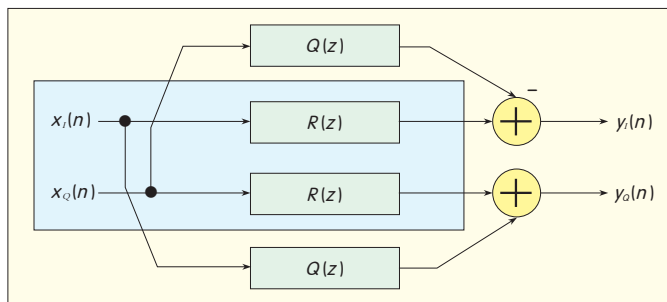


Figure 10. Physical implementation of a real digital filter (shaded) and complex digital filter applied to I/Q signals.

filters generally leads to impractically high filter orders. To overcome this problem, a multistage filtering structure was applied to the GDFT-FB to reduce the number of coefficients. Taking this approach, the number of filter coefficients and operations per input sample are reduced compared with the single-stage design. These reductions make the physical implementation more practical for fixed-point implementation using existing FPGA tools.

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Crest Factor Reduction for OFDM Using Selective Subcarrier Degradation

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Abstract: This paper describes a crest factor reduction (CFR) method that reduces peaks in the time domain by modifying selected data subcarriers within an OFDM signal. The data subcarriers selected for modification vary with each symbol interval and are limited to those subcarriers whose data elements are mapped onto the outer boundary of the constellation. In the proposed method, a set of peaks are identified within an OFDM symbol interval. Data subcarriers whose data element has a positive or negative correlation with the set peak are selected. For a subcarrier with an outer element and a significant positive correlation, a bit error (reversal) is intentionally introduced. This moves the data element to the opposite side of the constellation. Outer elements on negatively-correlated subcarriers are increased in magnitude along the real or imaginary axis. Experimental results show that selecting the correct subcarriers for bit reversals and outward enhancements reduces the peak-to-average power ratio (PAPR) of the OFDM signal to a target value and limits in-band degradation measured by bit error rate (BER) and error vector magnitude (EVM).

Keywords: crest factor reduction; OFDM; PAPR; wireless communication system; digital transmitter

1 Introduction

Orthogonal frequency-division multiplexing (OFDM) waveforms can have large peak-to-average power ratios (PAPR). Crest factor reduction (CFR) reduces peaks at the expense of signal quality. Usually, degradation is distributed throughout the signal's frequency bandwidth in the form of spectral leakage and in-band errors. However, because the OFDM signal is created in the Fourier domain, degradation can be concentrated to specific subcarriers (frequency bins of the FFT).

In the proposed method, CFR is used sparingly to bound the PAPR when transmitting at high power levels. This differs from the usual approach of maximizing PAPR reduction. The bound is met, and bit error rate (BER) is limited without deviating from the OFDM

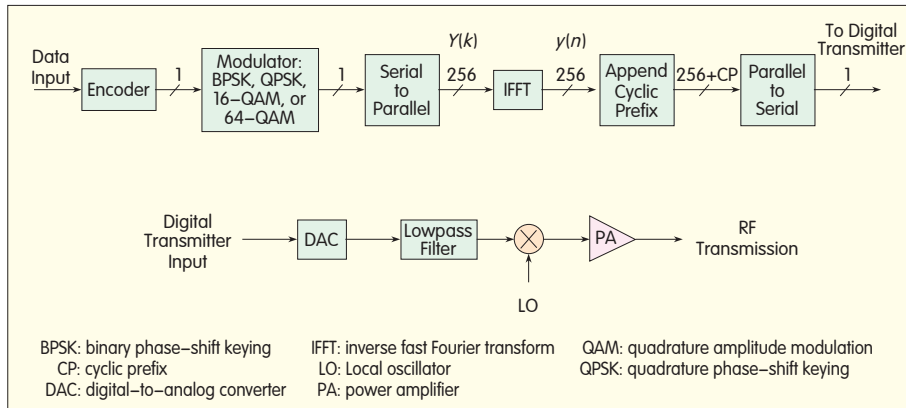
standard — for example, Worldwide Interoperability for Microwave Access (WiMAX) 802.16 [1]. This peak power bound allows the power amplifier (PA) in the transmitter to be designed for greater power-added efficiency (PAE) [2]. It may be necessary to enforce a second PAPR bound if the dynamic range of the digital-to-analog converter (DAC) cannot prevent clipping for all possible signals.

The remainder of this introduction describes OFDM signal generation as well as the subcarrier phase alignments that create peaks. Section 2 contains a review of CFR methods. Section 3 introduces new CFR methods for intentionally degrading selected subcarriers whose data elements are correlated (phase aligned) with the peaks of the OFDM signal. Section 4 contains experimental results that show a WiMAX signal can be crest-factor reduced to a target PAPR by

introducing an acceptable amount of in-band degradation. This degradation is measured by the BER and error vector magnitude (EVM).

1.1 OFDM Transmit Overview

Creation of an OFDM symbol for radio frequency (RF) transmission is shown in Fig. 1. The symbol is part of a data stream that has been 1) encoded, 2) modulated, 3) converted from serial to parallel as a 256 sample block, 4) converted to the time domain using an inverse fast Fourier transform (IFFT), 5) extended using a cyclic prefix (CP) to 256 + CP samples, and 6) converted back into a serial data stream. The data stream is then converted from DAC, lowpass filtered, up-converted to RF, then amplified by a PA. The signals $Y(k)$ and $y(n)$ are important for the crest factor method presented in this paper. These symbols correspond to the Fourier domain and time domain data



▲ Figure 1. RF transmission of one OFDM symbol [3].

blocks, respectively, of the OFDM symbol.

The encoding includes coders and interleavers to allow for error correction at the receiver. The modulator allows rate changes, and the rate is selected according to the received signal-to-noise ratio (SNR) and BER at the receiver. The rates from lowest to highest are binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), 16-quadrature amplitude modulation (16-QAM), and 64-QAM. In the serial-to-parallel conversion, a frequency domain representation is created, and the data elements are assigned to different subcarriers of the OFDM signal. The IFFT transforms the data from the frequency domain to the time domain. The cyclic prefix is a copy of the tail of the time domain block and is appended to the beginning of the time domain block. The cyclic prefix protects against intersymbol interference (ISI) caused by multipath RF propagation.

Within an OFDM symbol, the subcarriers may be data subcarriers, pilot subcarriers, or null subcarriers. No data elements are mapped onto the null subcarriers, which include the outer guard-band frequencies and the DC subcarrier. The pilots are BPSK-modulated and assigned to specific subcarriers. The remaining subcarriers are used for data transmission, which may be modulated using BPSK, QPSK, 16-QAM, or 64-QAM.

The OFDM-transmitted signal is a sequence of symbols sent as a

down-link (DL) subframe. This subframe comprises a preamble, frame control header (FCH), and DL bursts. QPSK is used for the preamble and BPSK for the FCH. BPSK, QPSK, 16-QAM, or 64-QAM (except for the BPSK pilots) is used for the DL bursts. The preamble and FCH are sent first, and the DL bursts are sent in order of the modulation rates (lower rates are sent first).

The OFDM symbol at the output is a time-domain data sequence. Although the individual data subcarriers are transmitted using simple modulation mappings, the magnitude in the time domain varies significantly. This is due to the IFFT operation that forms each time-sample from a sum of 200 random-phase variables (56 of the 256 subcarriers are null subcarriers). Phase alignment of subcarriers in the frequency domain results in large peaks in the time domain.

Peak-forming phase alignment in the frequency domain varies according to the position of the peak after the IFFT within the time block. A peak at time t_{peak} within the interval $t = [0, 255]$ is maximized by the following subcarrier phases:

$$\theta_{\text{align}(t_{\text{peak}})}(k) = -k \cdot \Delta\omega \cdot t_{\text{peak}} + \theta(t_{\text{peak}}) \quad (1)$$

where $\Delta\omega = \frac{2\pi}{N}$ ($N = 256$), k is the

subcarrier frequency index (DC = 0), and $\theta(t_{\text{peak}})$ is the phase of the complex time sample at t_{peak} .

The magnitude of the subcarriers also has an effect on peaking. Although the magnitude is constant for BPSK and

QPSK, it varies between constellation elements for 16-QAM and 64-QAM. Higher magnitudes are found at the outer elements of the 16-QAM and 64-QAM constellations. As a result, it can be assumed that many of these outer constellation elements are present in the data subcarriers when a large peak appears in the time domain.

2 Crest Factor Reduction

Large peaks cause problems because PAs become less efficient as the PAPR of the RF signal increases. Limiting the PAPR is necessary for a more efficient transmitter design. This process is called CFR. Past CFR methods for OFDM signals include clip and filter, partial transmit sequence (PTS), selective mapping (SLM), tone reservation, and constellation extension. The following is a summary of these CFR methods and their suitability for OFDM signals.

The direct CFR method involves clipping peaks of the time signal $y(n)$ when they exceed a specified level, L . The clipped signal $y_{\text{clip}}(n)$ is

$$y_{\text{clip}}(n) = \begin{cases} L \cdot \frac{y(n)}{|y(n)|} & \text{for } |y(n)| > L \\ y(n) & \text{otherwise.} \end{cases} \quad (2)$$

The excess peak waveform $y_{\text{peaks}}(n)$ becomes

$$y_{\text{peaks}}(n) = y(n) - y_{\text{clip}}(n). \quad (3)$$

Clipping moves the constellation elements from their assigned positions. The difference between the actual and assigned positions in the IQ space is called the constellation error or EVM. The allowable relative constellation error for WiMAX, averaged over subcarriers, frames, and packets, depends on the rate modulation where the most difficult specification is -31.0 dB for the 3/4 rate 64-QAM. Clipping tends to distribute excess peak energy over the 256 subcarriers, including the null and pilot subcarriers. As well as EVM limits on the data subcarriers, there are also limits on spurious emissions and adjacent channel leakage ratio (ACLR). These limits are specifically for the null subcarriers

within the guard-band frequencies. The energy from the clipped peaks must be constrained to reside primarily on the in-band subcarriers.

Filtering attenuates the excess peak energy present in the null subcarriers (except for the DC subcarrier). That is,

$$\Delta y(n) = \sum_{\tau} y_{\text{peaks}}(n - \tau) \cdot h(\tau) \quad (4)$$

where $h(\tau)$ is a filter kernel. The crest-factor-reduced signal being transmitted, denoted $y_{\text{CFR}}(n)$, becomes

$$y_{\text{CFR}}(n) = y(n) - \alpha \cdot \Delta y(n) \quad (5)$$

where α is a scaling term used to control the EVM introduced by the CFR [4], [5]. In some clip and filter implementations [6], the excess peak waveform $y_{\text{peaks}}(n)$ is replaced by a sequence of delta functions. Each delta function is located at a peak and assigned a magnitude and phase that match the excess value of the peak. This sequence is filtered using (4).

Using α in (5) for controlling EVM of OFDM signals is not effective because the EVM limit varies according to the function of the subcarrier and the rate modulation of the data (BPSK, QPSK, 16-QAM, or 64-QAM). It is beneficial for the receiver to have accurate pilot information, which means the CFR-induced EVM should be zero for pilot subcarriers. Multiaccess OFDM, such as OFDMA and LTE, may have different rate modulations on different subcarrier blocks. Because the allowable EVM is larger for BPSK and QPSK than for 16-QAM and 64-QAM, some researchers [7] convert the excess peak signal back into the frequency domain and apply the filtering and rate-dependent EVM control by weighting the subcarriers. The result is then converted back into the time domain to produce the desired $\Delta y(n)$ and $y_{\text{CFR}}(n)$.

The EVM control for a data subcarrier depends on the modulation type. CFR attempts to introduce EVM on data subcarriers to reduce peaks without increasing the BER at the receiver. Thus, QPSK allows more EVM than 64-QAM because the distance between neighboring points in the constellation is greater. However, some researchers [8] have exploited the fact

that points on the outer boundary of the constellation have no neighbors in the outward-expanding direction. As a result, EVM need not be limited in the outward direction because it does not cause bit errors at the receiver. Outward expansion is also used in the proposed CFR and is discussed in section 3.

In a different class of CFR methods, CFR disrupts the subcarrier phase alignments that create peaks. These methods include partial transmit sequence (PTS) [9]–[11] and selective mapping (SLM) [12]. The subcarriers are multiplied by a set of different phase-shift vectors that produce a set of potential time sequences. The time sequence with the lowest PAPR is transmitted. Information about the phase-shift vector used must be sent to the receiver to allow demodulation. This is considered a disadvantage of the method. A PTS method specifically for LTE and not requiring the phase-shift vector to be sent to the receiver is described in [13]. Neither PTS nor SLM is used in the proposed CFR method.

A third CFR method involves reserving some of the subcarriers as peak-reducers; that is, the reserved subcarriers do not carry any data. This method is called tone reservation [14], [15]. Once a peak is detected in the time domain, the magnitudes and phases of the reserved subcarriers are selected to reduce the peak. Unfortunately, data throughput is reduced because fewer data subcarriers are available. It is possible to use tone reservation as a form of clip and filter with EVM control. The EVM is set to zero for all data subcarriers that are not reserved for peak reduction. The scale factor, α , may have to be increased above unity for such an implementation in order to compensate for the sparseness of the reserved subcarriers in the frequency domain. Reserved tones are not used in the proposed CFR method.

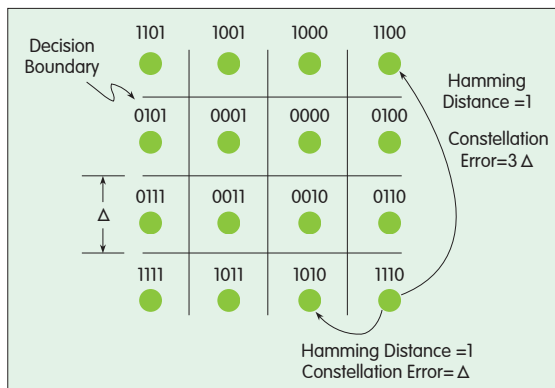
A fourth CFR method involves altering the constellation mapping so that elements are not unique. This is referred to as constellation extension [16]. A redundant mapping of input bits

is used so that opposing points on the constellation, $d_{i\alpha}$ and $-d_{i\alpha}$, represent the same data at the receiver. The advantage of constellation extension is that π radian phase shifts can be introduced onto some of the subcarriers with the goal of disrupting peak-forming phase alignments. The downside of this method is that one bit is lost in the constellation mapping, which reduces throughput for QPSK, 16-QAM, and 64-QAM to 1/2, 3/4, and 5/6 of the original value, respectively. Also, the Gray code mapping specified in the standard must be abandoned. The proposed CFR method similarly introduces large phase shifts onto selected subcarriers; however, the phase shifts are applied to the standard Gray code mapping instead of using the redundant constellation mapping already described.

3 Proposed CFR Method

The proposed CFR method does not alter the WiMAX (or other OFDM) standard nor does it require additional information to be sent to the receiver. The accuracy of the null and pilot subcarriers is preserved by restricting constellation errors to selected data subcarriers. CFR modifications are applied only to subcarriers whose data elements are mapped onto the outer positions of the constellation. For BPSK and QPSK, the outer elements include the entire constellation. For 16-QAM and 64-QAM, there are 12 (of 16) and 30 (of 64) outer elements, respectively. The outer elements have special properties in terms of constellation errors and BER. These properties are exploited in the proposed CFR method.

In a 16-QAM constellation, the IQ mapping and decision boundaries used by the receiver define the relationship between constellation errors and BER. The 16-QAM mapping is a Gray code (Fig. 2). Also shown in Fig. 2 are the decision boundaries of the receiver. It is of interest to determine a) the largest constellation error that can be tolerated without causing a bit error, and b) the largest constellation error caused by a single bit reversal. The number of bit reversals between



▲ Figure 2. 16-QAM constellation with Gray code mapping and decision boundaries. Outer elements can have different constellation errors for Hamming distance = 1.

the actual and received elements is referred to as the Hamming distance.

The largest constellation error that can be tolerated without causing a bit error depends on the position of the data element. A single bit error occurs when the constellation error causes the received element to cross one of the horizontal or vertical boundaries. The distance between an interior element and the closest boundary is $\Delta/2$; however, this allowable error, which includes additive noise, is shared between the transmitter, receiver, and propagation channel. For the outer elements, there is at least one direction where no decision boundary exists: the outward direction away from either the I axis or Q axis (depending on the position within the constellation). At the corner elements, there are two directions unconstrained by decision boundaries. Intentionally increasing the constellation errors for outer elements in these unconstrained directions does not increase the BER [6].

To determine the largest constellation error caused by a single bit reversal, we need to look at the Gray code mapping. Neighboring elements in the horizontal and vertical directions have a Hamming distance of one. If we assume the actual and received constellation elements differ by a Hamming distance of one, the constellation error for an interior point is Δ . For outer elements, a Hamming distance of unity can produce a constellation error of 3Δ (Fig. 2). Thus, large constellation errors can be created from a single bit

reversal on an outer element.

Using the CFR method, constellation errors are created. The proposed method concentrates the constellation errors on the data subcarriers that produce the least amount of BER. That is, the goal is to generate as much constellation error as necessary for the CFR while creating the minimum Hamming distance between the actual and received elements. Data subcarriers with outer constellation elements are ideal for CFR.

Two CFR methods are possible: outward enhancement and bit reversal. The former increases the I- or Q-component magnitude for all data subcarriers that have an outer element and negative correlation to the peak. The latter reverses the sign of the I- or Q-component for subcarriers that have an outer element and large positive correlation to the peak. Because sign reversal causes a bit error, it is used more sparingly than outward enhancement.

As well as reducing the peak value, it is also important not to significantly increase the secondary peaks in the time block. To avoid enhancing secondary peaks, certain subcarriers cannot be used for peak reduction. Only subcarriers with a negative correlation to the primary peak and all secondary peaks are used for the outward enhancements. Only subcarriers with a positive correlation to the primary and secondary peaks are

considered for bit reversal. The number of secondary peaks specified must be limited to avoid eliminating too many subcarriers from the CFR process.

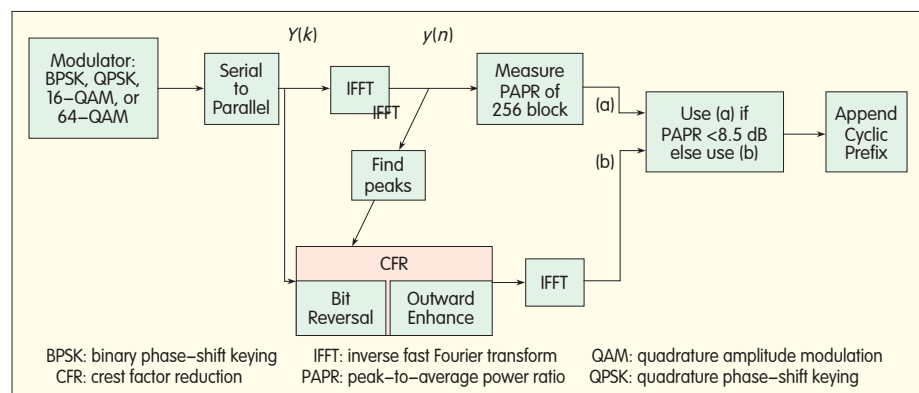
The CFR method is shown in Fig. 3. The OFDM system in Fig. 1 is modified so that the PAPR is measured in the time domain, after the IFFT and before the addition of the cyclic prefix. If the PAPR is small enough (less than 8.5 dB for example), the original OFDM data block is used for transmission. If the PAPR is too large, the CFR OFDM data block is used. Before CFR is applied, the primary and secondary peaks are identified within the time block. The CFR module reduces the primary peak and does not increase the secondary peaks. CFR is applied in the Fourier domain. The CFR signal is then converted to a time block using an IFFT. The CFR OFDM data block is not computed when the PAPR of the original signal $y(n)$ is below 8.5 dB.

The CFR module is shown in greater detail in Fig. 4. CFR uses the phase alignment profile described by (1) for each of the primary and secondary peaks. The phase alignment profile is cross-correlated with the real and imaginary components of the subcarriers containing outer elements. The cross correlations for t_{peak} are

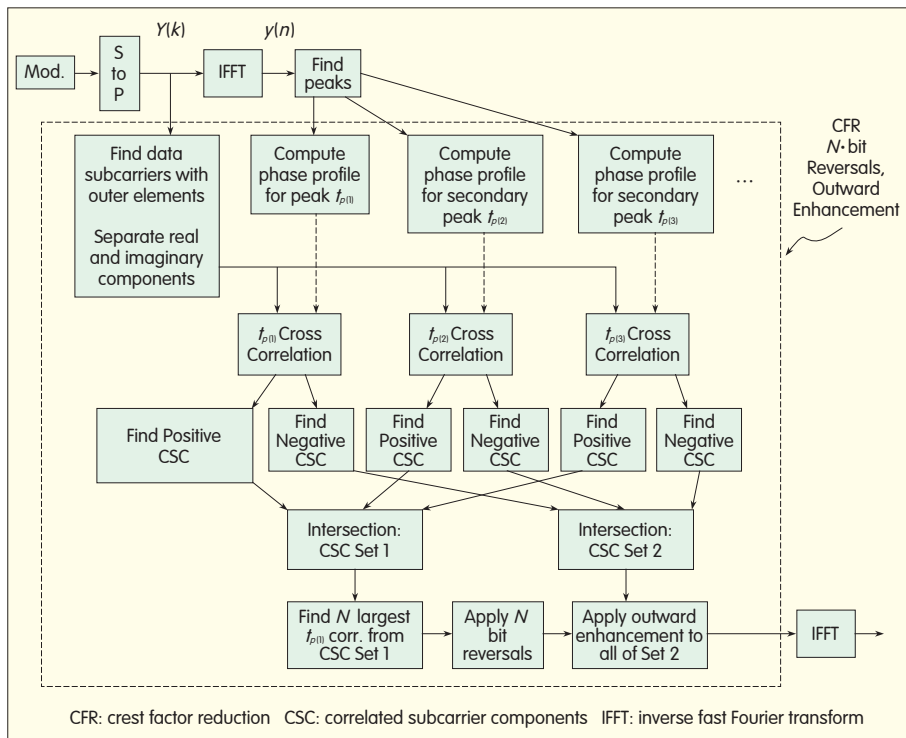
$$C_{\text{Re}}(k; t_{\text{peak}}) = \text{Re}\{Y(k)\} \cdot \cos\{\theta_{\text{align}(t_{\text{peak}})}(k)\} \quad (6)$$

$$C_{\text{Im}}(k; t_{\text{peak}}) = \text{Im}\{Y(k)\} \cdot \sin\{\theta_{\text{align}(t_{\text{peak}})}(k)\}. \quad (7)$$

The peak is formed by the sum of many subcarriers. Because of the phase term $\theta(t_{\text{peak}})$ in (1), subcarriers with positive cross-correlations contribute to the peak whereas those with negative cross-correlations



▲ Figure 3. CFR Schematic [3].



▲ Figure 4. CFR for the case of N bit reversals per OFDM symbol plus outward enhancement [3].

attenuate the peak. Applying a bit reversal, that is, changing the sign of either $\text{Re}\{Y(k)\}$ or $\text{Im}\{Y(k)\}$ to a subcarrier, reverses the cross-correlation. A positive to negative change reduces the peak. Increasing the magnitude of either $\text{Re}\{Y(k)\}$ or $\text{Im}\{Y(k)\}$ for a subcarrier possessing a negative cross-correlation also reduces the peak. Thus, a coordinated effort to create or enhance the negative cross-correlation on many subcarriers results in effective CFR.

There is a risk that a secondary peak will increase in response to the CFR of the primary peak. It would be poor use of bit reversals and outward enhancements if the CFR transformed a secondary peak into a primary peak. To prevent this, the cross-correlations are computed relative to the secondary peaks as well. The intersection of the sets of positively-correlated components for each peak is used as a pool of available subcarriers for a bit reversal. The available subcarrier possessing the largest positive correlation to the peak is selected. The intersection of the

negatively-correlated components for each peak is also computed. The outward enhancement is applied to all the available subcarrier components from the negatively-correlated set. The enhancement is a scalar multiple of the original value, for example, $1.05 \text{Re}\{Y(k)\}$ or $1.05 \text{Im}\{Y(k)\}$.

In this approach, a secondary peak has a magnitude that is above a threshold defined as a fraction of the primary peak. The fraction is determined by the amount of peak reduction sought from the CFR. The potential increase in the secondary peak is directly related to the decrease in the primary peak. Currently, the target PAPR is set to 8.5 dB. When the original PAPR is greater than 8.5, 9.2, or 9.7 dB, the fractional thresholds for secondary peaks are 0.85, 0.8, and 0.75 of the primary peak, respectively. These thresholds were obtained by experimentation.

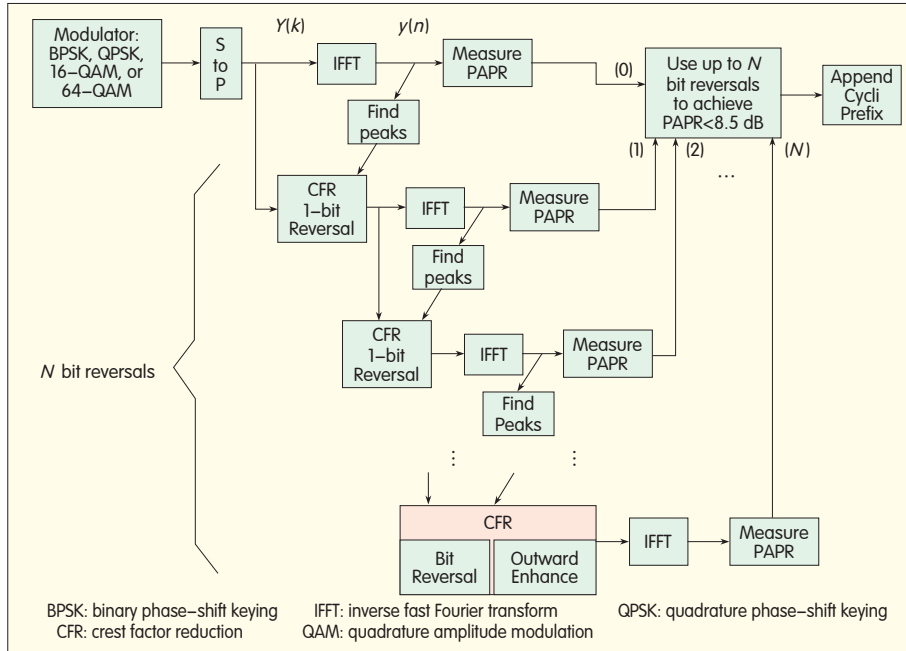
Selecting too many secondary peaks can be problematic because the intersection of the correlated subcarrier component sets (Fig. 4) may become a null set, preventing any CFR. To avoid this problem, the fractional threshold for

secondary peaks is raised, if necessary, until the number of selected peaks is three or less. For these rare occurrences, the number of bit reversals is reduced to avoid excessively enhancing the secondary peaks, but this comes at the expense of increased PAPR. Thus, to limit the number of secondary peaks considered, it is sometimes necessary to increase the target PAPR for a given block, even if this results in clipping at the PA.

Because a bit reversal typically reduces the peak by about 0.4 dB, it is necessary to specify additional bit reversals for large peaks. The number of bit reversals for an OFDM symbol is 1, 2, 3, or 4 when the original PAPR exceeds 8.7, 9.2, 9.7, and 10.1 dB, respectively. There are two approaches to implementing N bit reversals when $N > 1$. Either all N bit reversals are applied at once (Fig. 4), or single-bit reversals are applied recursively N times (Fig. 5). For $N = 0$ (PAPR < 8.7 dB), only outward enhancement is used.

Single bit reversal applied recursively N times is shown in Fig. 5. This approach requires additional IFFTs to be computed. Because the primary and secondary peaks are re-computed after each bit reversal, the fractional threshold for the secondary peaks is set to 0.85. Outward expansion is applied after the last bit reversal has been completed.

In addition to bit reversals and outward expansions, a third CFR approach can be used. In this approach, constellation error is distributed over all elements, not just the outer elements. The phase profiles for the primary and secondary peaks are multiplied by a scalar term and then added to the Fourier coefficients. This introduces constellation errors similar to clipping, except that the affected subcarriers are selected, which allows the pilot and null subcarriers to be transmitted without error. Because the phase profiles of the primary and secondary peaks have already been computed (Fig. 4), the additional computational cost is minimal. The size of the scalar term controls the



▲ Figure 5. CFR for N bit reversals per OFDM symbol plus outward enhancement using the recursive implementation [3].

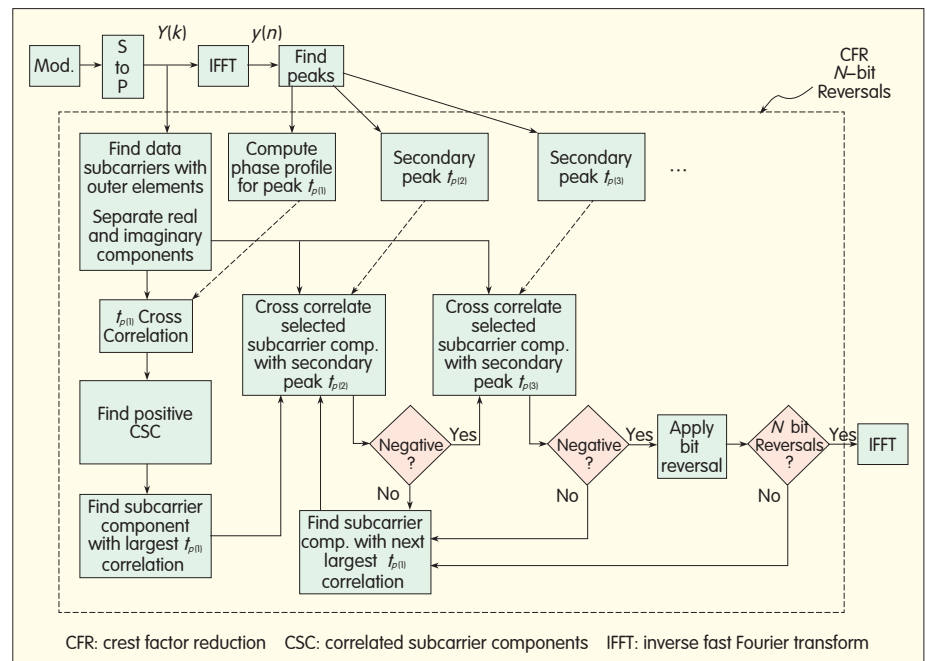
constellation error in this third part of the CFR, and the scalar term is typically selected to be small in value. That is, this is not the primary source of peak reduction. In the proposed CFR method, the third approach is used to assist with reducing the largest peaks. The scale term is made to be an increasing function of the PAPR of the OFDM symbol.

In the CFR approach shown in Fig. 4, the cross-correlation is computed for all subcarrier components associated with the primary and secondary peaks. If only bit reversals are used for CFR, the cross-correlation for the secondary peak need only be computed for the subcarrier components associated with the primary peak (Fig. 6). This can be thought of as a serial implementation of a correlated subcarrier component search (Fig. 4), which requires fewer computations on average because the set of available subcarrier components becomes smaller as subsequent secondary peaks are tested.

4 Results

The CFR approach in Fig. 4 is applied to a WiMAX DL subframe comprising two QSPK symbols for the

preamble, one BPSK symbol for the FCH, and 75 64-QAM payload symbols. The 64-QAM symbols contain BPSK pilot subcarriers. The ratio for the cyclic prefix is 0.125, which corresponds to 32 time samples for the 256 data blocks. The DL subframe is



▲ Figure 6. Serial implementation of the correlated subcarrier component search, suitable for CFR using bit reversals only [3].

repeated 20 times with random data sent on the data subcarriers.

BER associated with the CFR is caused by the bit reversals only and does not account for the forward error correction (FEC) provided by the bit encoding. The EVM caused by the CFR is measured with

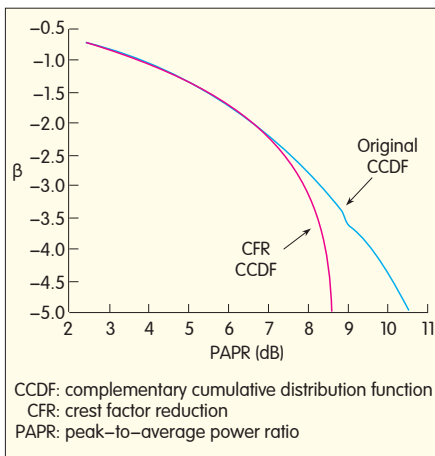
$$EVM = \sqrt{\frac{E[|d_{IQ}(n) - d_{CFR}(n)|^2]}{E[|d_{IQ}(n)|^2]}} \quad (8)$$

where $E[\]$ is expected value, and d_{IQ} and d_{CFR} are the data elements within the IQ constellation space before and after CFR, respectively. EVM is measured in two ways: the first uses the original constellation data point for $d_{IQ}(n)$ whereas the second defines $d_{IQ}(n)$ as the nearest constellation point to $d_{CFR}(n)$. In the first way, in-band signal degradations associated with both the outward expansion and bit reversals are measured; in the second way, degradation associated with the outward expansion only is measured.

CFR has a target PAPR of 8.5 dB. The PAPR is defined as

$$PAPR = \frac{\max(|y(t)|^2)}{E[|y(t)|^2]} \quad (9)$$

where $y(t)$ is the analog output signal



▲ Figure 7. CCDF for the original and crest factor reduced WiMAX time waveforms. The vertical axis represents the 10^β probability that the signal power $|y(n)|^2$ exceeds the level $P_o = \text{PAPR} \cdot P_{\text{ave}}$, where P_{ave} is the average signal power.

after filtering. In practice, however, the PAPR is defined using the digital time domain signal $y(n)$ and is based on the signal power statistics rather than the absolute peak. The practical peak is the level P_o , for which the signal power $|y(n)|^2$ has a 10^β probability of exceeding this peak. The complementary cumulative distribution function (CCDF) of $|y(n)|^2$, in which β is plotted as a function of P_o , is a useful description of the signal. In this paper, two probability thresholds are selected for defining the signal peak: $\beta = -4$ and -5 .

The CCDFs of the original and crest-factor-reduced OFDM time sequences are shown in Fig. 7. Using the 10^{-4} probability threshold for the CFR OFDM time sequence, PAPR is 8.42 dB, which is a reduction of 1.2 dB from the 9.62 dB PAPR of the original signal. Using the 10^{-5} probability threshold, PAPR of the CFR and original OFDM time sequences are 8.56 dB and 10.54 dB, respectively. That is, CFR reduces PAPR by 2 dB when the 10^{-5} threshold is used. The crest-factor-reduced waveform meets the target PAPR of 8.5 dB for the 10^{-4} probability threshold, which is used more commonly in PA design than the 10^{-5} threshold.

The BER introduced by the CFR is 0.00019 (327 bit reversals from

1730460 bits sent). The EVM, including the bit reversals, is 0.0725, which is high for 64-QAM. The limit for 3/4 rate 64-QAM is 0.0282. However, when using the easier measure that excludes the contribution from bit reversals, EVM is 0.0119. This EVM level is considered acceptable. Most of the EVM for this second measure is due to the outward expansion of the constellation, which does not increase BER at the receiver.

This approach does not involve trying to achieve the lowest CFR. Instead, a bounded CFR is created to ease the design of the PA and digital circuitry and to generate a low BER. With this type of CFR, 90% of the CFR symbols are transmitted without modification. For such pass-through cases, only the PAPR measurement is required, and no additional IFFTs are computed.

5 Conclusion

A CFR method that is suitable for WiMAX and other OFDM signals has been presented. Degradation associated with CFR is restricted to selected data subcarriers whose data elements are mapped onto the outer boundary of the IQ constellation. Subcarrier components correlated to the phase profiles of the primary and secondary peaks are identified for modification by outward expansions and bit reversals. The peak-to-average power for the WiMAX signal is reduced to a target level, and this allows the PA in the transmitter to be designed for high PAE. CFR is achieved with an acceptable amount of in-band BER and EVM degradation.

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Biography

R. Neil Braithwaite (nbraithwaite@pwav.com) received his B.Sc. degree in electrical engineering from the University of Calgary in 1985. He received his M.Sc. and Ph.D. degrees from the University of British Columbia in 1989 and 1992. From 1992 to 1995, he conducted postdoctoral research at the University of California, Riverside. From 1985 to 1987 and 1995 to 2002, he worked for Computing Devices Company (Canada), Nortel (Canada), and Agilent Laboratories (USA). Since 2002, he has been working for Powerwave Technologies (USA). He is the author of several papers and patents, as well as a recent book chapter on digital predistortion in RF power amplifiers [17].

An Antenna Diversity Scheme for Digital Front-End with OFDM Technology

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Abstract: In this paper, we propose a new antenna diversity scheme for OFDM-based wireless communication and digital broadcasting applications. Compared with existing schemes, such as post-fast Fourier transform (FFT), pre-FFT, and polyphase-based filter-bank, the proposed scheme performs optimally and has very low computational complexity. It offers a better compromise between performance, power consumption, and complexity in real-time implementation of the receivers of broadband communication and digital broadcasting systems.

Keywords: OFDM; digital front-end; MIMO; cross-layer processing; diversity; antenna

1 Introduction

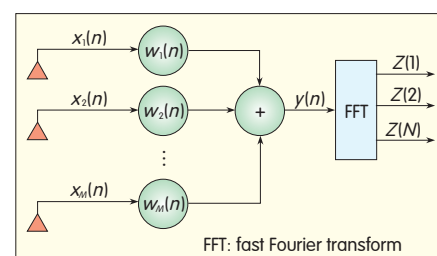
In modern wireless broadband communication and digital broadcasting, orthogonal frequency-division multiplexing (OFDM)-based modulation schemes are usually used. However, an OFDM system has very poor reception when there is noise, interference, or moving objects. To solve this problem, many technologies have been proposed and used in real applications [1], [2]. Among these technologies, beamforming-based diversity technology is the most promising. It uses multiple antennas at the receiver side and spatial filtering to optimize reception in noisy and mobile environments. Figs. 1, 2, and 3 show three representative solutions: pre-fast Fourier transform (pre-FFT), polyphase filter-bank, and post-FFT [1], [4], [5], [7], [8].

In Fig. 1, $X_1(n)$, $X_2(n)$, ..., $X_M(n)$ are the received signals in one of M antennas, and $W_1(n)$, $W_2(n)$, ..., $W_M(n)$ are the weights applied to these

antenna signals. All the weighted signals are summed to one channel, such as one antenna's output and then forwarded for further FFT processing, which is required in any OFDM-based receiver. These weights are designed to meet an optimization criterion, and the most common criterion is the maximum ratio combination (MRC). With MRC, the optimized weight vector, $\mathbf{W}(n) = [W_1(n), W_2(n), \dots, W_M(n)]$, can be obtained by

$$\mathbf{W}_{\text{opt}}(n) = E[X(n) \times Y(n)] \quad (1)$$

where $\mathbf{X}(n) = [X_1(n), X_2(n), \dots, X_M(n)]$ and $y(n) = \mathbf{W}^H(n)\mathbf{X}(n)$. Pre-FFT can give 5–10% gain in bit-error reduction



▲ Figure 1. Pre-FFT scheme [1].

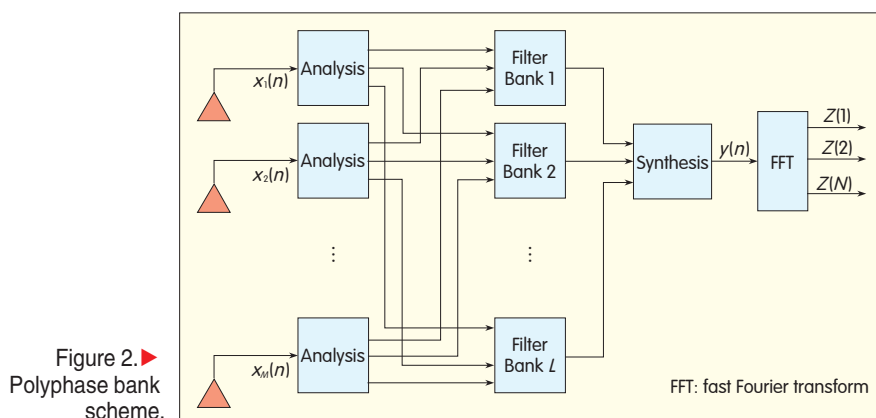
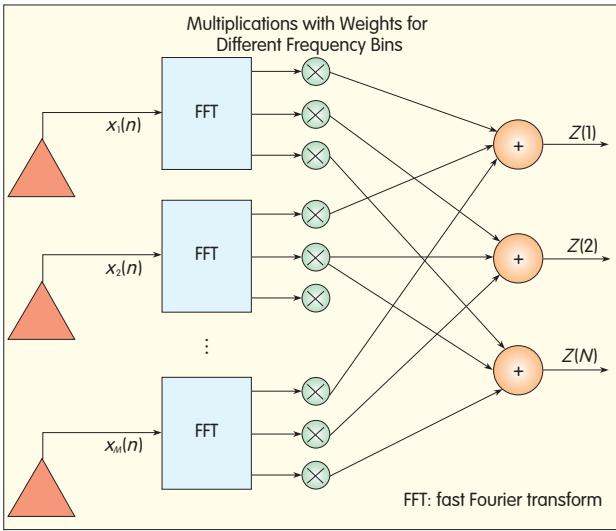


Figure 2. ▶ Polyphase bank scheme.



▲ Figure 3. Post-FFT scheme [1].

and is not complex in implementation. However, this processing is done only in the time domain, and the same weights are used over the entire frequency band (all-carriers). Because of the shortcomings of simple pre-FFT, a polyphase filter bank scheme is proposed (Fig. 2).

In a polyphase scheme, each antenna signal is divided into a number of frequency band signals, and different weights apply to different bands. This scheme can further improve performance at the cost of increased computational complexity that arises as a result of multichannel antenna signal decomposition (analysis) and multiplication of weights in each channel. Different weights in different frequency bins and bands can be used in the frequency domain, and this is called post-FFT (Fig. 3).

A polyphase scheme is a special case of post-FFT. Post-FFT performs the best but has the greatest computational complexity. Pre-FFT has the least computational complexity but improves performance the least. Another approach is to divide M antennas into L groups. Each group uses pre-FFT and obtains L outputs. With these L outputs, post-FFT is then used to obtain the desired outputs. Compared with the full post-FFT scheme, this alternative avoids $M-L$ FFT computations at the cost of reduced performance. A diversity

scheme that provides a better compromise between performance, complexity, and power consumption is highly desired.

2 The Proposed Scheme

Here, we propose a new scheme in which the number of variables computed is reduced from $N \times M$ (in post-FFT) to $N+M$. The scheme shown in Fig. 4 performs just as well as the post-FFT scheme.

M antenna signals are weighted by the corresponding weight as the processing made in the pre-FFT algorithm in Fig. 1. These M weighted signals are added together to pass through an N -tap finite impulse response (FIR) eigenfilter, after which they are input for FFT processing. The number of unknown variables in the proposed scheme is $N+M$, which is significantly less than the $N \times M$ needed in post-FFT. Furthermore, only one FFT operation is needed in the proposed scheme instead of M FFT operations in the post-FFT scheme. Here we will prove that the post-FFT scheme in Fig. 3 and the proposed scheme in Fig. 4 give the same frequency-domain outputs, $Z(1), Z(2), \dots, Z(N)$. Using the optimization criterion in post-FFT, the variable matrix, $\mathbf{W}_{N \times M}$ in Fig. 3 can be rewritten as

$$\mathbf{W}_{N \times M} = [\mathbf{W}_{N,1}, \mathbf{W}_{N,2}, \dots, \mathbf{W}_{N,M}] = \mathbf{W}_C [C_1, C_2, \dots, C_M] \quad (2)$$

where $\mathbf{W}_{N,i}$ is the i th column of the $N \times M$ matrix and denotes the weights after FFT processing of the i th antenna in Fig. 3. \mathbf{W}_C is an N -dimensional vector, and C_i is a scalar (corresponding to each antenna). This suggests that Figs. 3 and 5 give the same outputs.

Because each block in Fig. 5 is linear processing, changing the order of the blocks results in the same performance. Hence, the scheme in Fig. 4 is obtained.

Now we determine the $N+M$ weights in proposed scheme.

\mathbf{W}_E , \mathbf{X}_h , and \mathbf{X}_t denote the weight vector of the eigenfiltering, the sequence of the head-guided interval, and the tail of the symbols, respectively. If the norm is a constant (unity, for instance), the weight vector is obtained in such a way that the error is minimized. That is,

$$\min \mathbf{W}_E^H E \|\mathbf{W}^H \mathbf{X}_h - \mathbf{W}^H \mathbf{X}_t\|^2 \\ \text{St. } \|\mathbf{W}^H \mathbf{W}\|_2 = 1. \quad (3)$$

According to beamforming matrix theory [3], the solution to the optimization problem is the eigenvector (minor component) corresponding to the smallest eigenvalue of the correlation matrix R , which is

$$E[(\mathbf{X}_h - \mathbf{X}_t)(\mathbf{X}_h - \mathbf{X}_t)^H]. \quad (4)$$

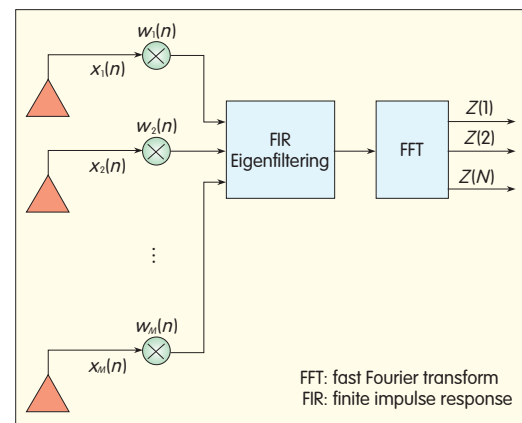
This is also the reason that the filtering in Fig. 4 is called eigenfiltering. In practical implementation, the minor component in the following adaptive algorithm can be updated:

$$\mathbf{W}(t+1) = \mathbf{W}(t) + \gamma s(t)(\mathbf{X}_h - \mathbf{X}_t - s(t)\mathbf{W}(t)) \\ s(t) = \mathbf{W}^H(t)(\mathbf{X}_h - \mathbf{X}_t) \quad (5)$$

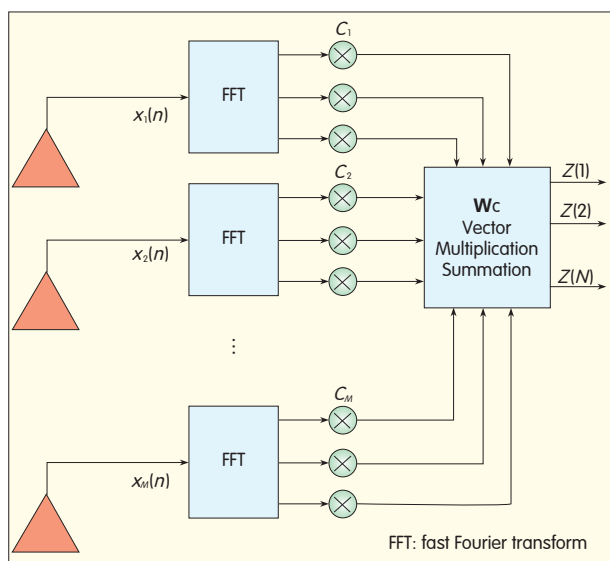
where γ is a constant. This algorithm is as complex as LMS algorithm, and the required multiplications are only on the order of N . An algorithm, such as MRC used in pre-FFT, can be used to determine the weights applied to each antenna before eigenfiltering.

3 Comparison and Discussion

Compared with existing solutions, the



▲ Figure 4. Proposed scheme.



▲ Figure 5. Alternative scheme for post-processing.

proposed scheme has the following features:

- The parameters to be computed in a real-time implementation are reduced from $M \times N$ to $N + M$, and performance remains the same as that of post-FFT.

- Only one FFT operation is needed instead of multiple FFT computations or polyphase filtering analyses. Table 1 shows computational complexity for various standards.

- The related parameters can be adaptively updated from the received samples of the each antenna. The adaptive algorithm used is as simple as the LMS algorithm, which has the computational complexity on the order of the number of unknown parameters.

With these features, the proposed scheme is a new tool for improving reception quality in broadband wireless communications and digital broadcasting. It will have very many practical uses in devices.

4 Conclusions and Future Work

In this paper, we have proposed a new and efficient diversity scheme for OFDM-based receivers. We have also shown the accuracy and effectiveness of the proposed scheme. When embedding this algorithm into real silicon, it is often desirable that one

platform support all existing standards (and their various modes) with high power efficiency, low cost, and short time to market [9]. Traditional integrated circuit technologies, such as application-specific integrated circuits (ASICs) and digital signal processors (DSPs), are not highly flexible and power efficient. An ASIC solution gives high performance with low power consumption and price, but it cannot support multiple standards nor is it sufficiently flexible. A DSP

is highly flexible but performs poorly and consumes much power. It may include high-speed arithmetic operations, such as multiply-accumulate, but the algorithms require extensive programming and more parallelism

than can be offered by a general DSP.

One alternative is to use a general DSP or reduced instruction set computing (RISC) processor plus hardware accelerators that are designed and optimized to implement FFT algorithm as well as eigenfiltering and its adaptive algorithm. In other words, an eigenfiltering unit performs a basic filter computation, an FFT unit performs FFT computations, and an adaptive unit implements the operations defined by (5) in section 2. These optimized accelerators may meet performance goals, but the accelerators are very narrow in their applicability, and this significantly reduces the flexibility of the processor-based solution.

An alternative that offers flexibility and parallelism is devices with FPGAs. These devices may combine processors with a programmable array of low-level logic devices, but they are expensive, and performance is limited at high temperatures.

In a future paper, we will introduce

➔To P.41

▼ Table 1. Parameters related to implementation of FFT in different standards

Standard	ISDB-T	DVB-H	DVB-T	FLO	CMMB	DTMB	T-DMB	WiMAX (Mobile)	WiMAX (Fixed)
FFT Size	256	2048	2048	4096	1024	1024	256	128	256
	512	4096			4096	4096	512	512	
	1024	8192	8192				1024	1024	
	2048						2048	2048	
	4096								
	8192								
Duration (μ s)	252	224	224	738.0	409.6	500	250	91.4	64
	504	448		2					
	1008	896	896						
Single FFT Cycles (k)	2.56						2.56	1.12	2.56
	5.76						5.76	5.76	
	12.8				12.8	12.8	12.8	12.8	
	28.2	28.2	28.2				28.2	28.2	
	61.4	61.4		61.4	61.4	61.4			
Symbol Number (K)	133.12	133.1	133.1						
	4	4.5	4.5	1.4	2.4	2	4	11	15.63
	2	2.2							
MIPS	1	1.1	1.1						
	10.24	127	127	83.2	30.72	25.6	10.24	12.3212	40.01
	11.52	135					23.04	63.36	
	12.81	146	146		147.00	132.8	51.20	140.80	
	23.04						112.2	310.20	
	25.60								
	28.20								
	112.80								
	132.80								
	133.12								
CMMB: China Mobile multimedia broadcasting DTMB: digital terrestrial multimedia broadcast DVB-H: digital video broadcasting-handheld DVB-T: digital video broadcasting-terrestrial FFT: fast Fourier transform									
FLO: forward link only ISDB-T: integrated services digital broadcasting-terrestrial MIPS: Million Instructions Per Second T-DMB: digital multimedia broadcasting via terrestrial									

A Histogram-Based Static-Error Correction Technique for Flash ADCs

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Abstract: High-speed, high-accuracy data converters are attractive for use in most RF applications. Such converters allow direct conversion to occur between the digital baseband and the antenna. However, high speed and high accuracy make the analog components in a converter more complex, and this complexity causes more power to be dissipated than if a traditional approach were taken. A static calibration technique for flash analog-to-digital converters (ADCs) is discussed in this paper. The calibration is based on histogram test methods, and equivalent errors in the flash ADC comparators are estimated in the digital domain without any significant changes being made to the ADC comparators. In the trimming process, reference voltages are adjusted to compensate for static errors. Behavioral-level simulations of a moderate-resolution 8-bit flash ADC show that, for typical errors, ADC performance is considerably improved by the proposed technique. As a result of calibration, the differential nonlinearities (DNLs) are reduced on average from 4 LSB to 0.5 LSB, and the integral nonlinearities (INLs) are reduced on average from 4.2 LSB to 0.35 LSB. Implementation issues for this proposed technique are discussed in our subsequent paper, "A Histogram-Based Static-Error Correction Technique for Flash ADCs: Implementation Aspects."

Keywords: Calibration; flash ADC; offset; trimming; uniform distribution

1 Introduction

An analog-to-digital converter (ADC) is an essential part of an RF receiver, but in many systems, an ADC limits performance.

To relax the dynamic range requirements of an ADC, a voltage gain amplifier (VGA) and filters (for adjacent-channel blocking) are used before the ADC. Typically, linear analog filters with sharp transition bands and good VGA designs are used. Such filters are difficult to implement, especially in an integrated system and in newer CMOS technologies. The design of these blocks should be simplified, and more should be required of the ADCs. In today's cellular applications, the main challenge is to reduce analog complexity as much as possible and shift it to the digital part of the system that relies on digital signal processing

(DSP). Analog complexity is reduced by minimizing the number of (mostly) discrete elements, such as high-Q filters, and lowering the number of analog cascaded stages in down-conversion. Reduction in analog complexity allows the system to be more integrated and makes it more compatible with a system-on-chip (SOC) design.

An important factor in ADC design is the power-accuracy trade-off. This is more critical in cellular applications, where portability significantly affects power consumption, especially that of the converter. A highly dynamic range in the converter is sometimes achievable at the cost of high power consumption. Calibration optimizes the power-accuracy trade-off, and the desired accuracy can be obtained with reduced power consumption. By reducing analog complexity and increasing digital complexity, calibration makes the converter more

conductive to process-scaling and more compatible with newer CMOS technologies. However, this comes at the cost of increased digital complexity because a larger part of the ADC is digital rather than analog.

In this paper, we focus on flash ADCs with low to moderate resolutions, that is, 3 to 8 bits. These resolutions are used extensively as the sub-ADC part of sigma-delta ADCs, in pipelined ADCs, or in applications ultrawideband where low resolution and very high-speed converters are needed. In a standard DCS-1800 for a low-IF receiver, a high-resolution, low-bandwidth converter is required. Such a converter can be realized using a sigma-delta ADC.

The accuracy of a flash ADC is mainly affected by the offsets of its comparators and references. To improve accuracy, components that are well-designed and comparatively large in terms of area and power are

commonly used. This results in higher cost and, perhaps more importantly, longer design time and limited process-scaling if the ADC is embedded in a system on chip (SOC).

In addition to the material presented in this paper, we give a more detailed analysis of the histogram-based static-error correction technique in [1], taking implementation issues into account. We study the transistor-implementation of a 5-bit, 1 GHz ADC in a 1.2 V, 65 nm CMOS process, and we evaluate the improvement in performance brought about by the calibration technique. We also suggest further improvements to the analog design so that analog complexity is further reduced in favor of digital complexity.

1.1 Calibration

Calibration techniques for flash ADCs have been reported in [2]–[6]. In most of these techniques [2]–[4], [6], the analog part — especially the high-speed analog signal path — of the flash converter is affected by the calibration circuitry. In some of these techniques [3], [4], offset compensation (trimming) is performed inside the comparator structures. In [3], trimming is performed by adjusting the internal resistive loads of the comparator preamplifiers. However, these loads are often difficult to trim accurately because of their high gain and nonlinearity, and trimming might be inefficient. In [2] and [6], linear trimming is performed efficiently by adjusting the voltages generated by the reference ladder. In [2], an accurate digital-to-analog converter (DAC) generates a calibration signal, but the design of such a DAC still has a high degree of analog complexity. In [6], each comparator is chosen sequentially and calibrated. This affects the main ADC structure; specifically, extra calibration circuitry affects the high-speed input signal path. In [5], trimming is performed by adjusting the bulk voltages of the comparator input transistors to keep the high-speed signal path intact. However, the trimming is nonlinear because of the nonlinear relationship between the bulk and threshold

voltages of the MOS transistor.

1.2 Algorithm Example

A histogram-based calibration technique for flash ADCs is an example of an error-correction technique for front-end ADCs. The theory of histogram test methods is well-known [7]–[13], and in this paper, a histogram method is used to extract the equivalent input-referred offset of each comparator in the flash ADC. This is an estimation process. Trimming is then performed by adjusting the reference voltage levels in order to compensate for the static error sources. The estimation process is fully digital, and no changes are made to the comparator structure. Trimming is performed by adding arrays of analog switches that are connected to the reference taps of the comparators so that the high-speed signal path of the converter is not affected.

To illustrate the calibration technique, behavioral-level simulations can be performed. Individual error sources can then be isolated, and their effects can be analyzed separately. In [1], a transistor-level ADC that uses the calibration technique is described, and practical implementation issues are discussed.

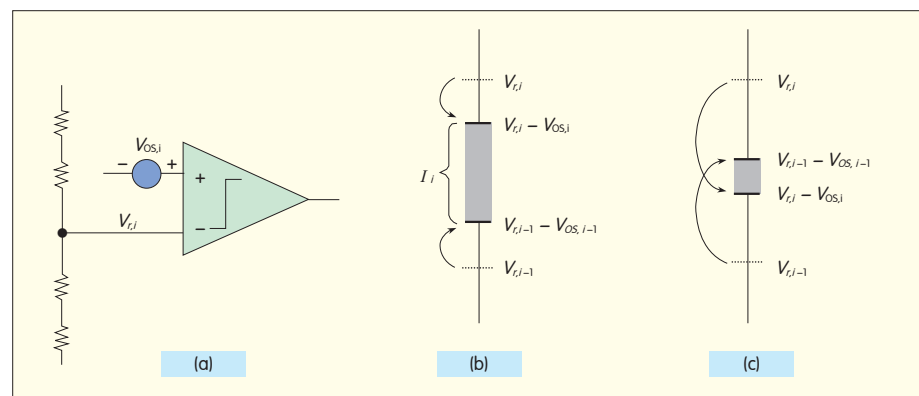
In section 2, main sources of static error are modeled. In section 3, the calibration technique is described, and in section 4, the estimation process is described in mathematical detail. In section 5, the trimming process and related practical issues are discussed. In section 6, simulation results are

given. Section 7 concludes the paper.

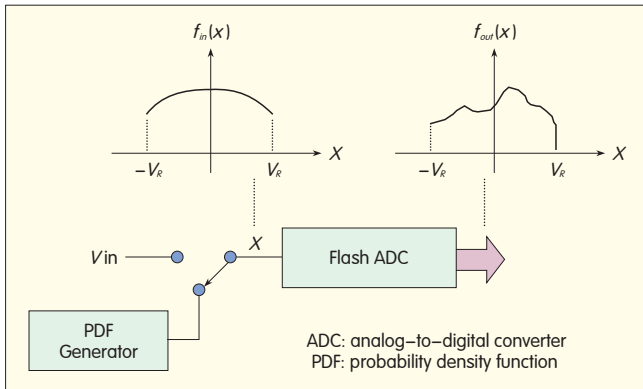
2 Examples of Static Errors

In an n -bit flash ADC, $2^n - 1$ reference levels are commonly generated by a resistor ladder. For each reference level, a comparator is used. The comparators compare the input signal with the reference levels, and combined, the comparators generate a thermometer code at their outputs. A digital decoder that filters out sparkle errors is usually used. Static errors affect the accuracy of the decision levels in the converter. Errors in the reference levels are mainly caused by resistor mismatch and comparator offsets. These two errors can be modeled (and combined) as a voltage source, V_{os} , at the input of each comparator, as shown in Fig. 1(a). For a low-resolution ADC, the matching of the resistors is usually much better than the nominal resolution of the flash converter, so the reference voltages from the resistor ladder can be treated as ideal values [6]. However, this is not the case for higher-resolution flash ADCs.

In Fig. 1(a), the comparator is assumed to be ideal, and the error voltage, V_{os} , in practice would be described by statistical variation over many individuals. This is shown in Fig. 1(b), where $V_{r,i}$ is the ideal reference level of the i th comparator, and $V_{os,i}$ is the corresponding offset voltage source of the ideal reference. The i th interval between two adjacent reference levels is denoted I_i . In an ideal converter, the



▲ Figure 1. (a) Static errors with voltage sources, $V_{os,i}$, and their effects for (b) small and (c) large offsets.



◀ Figure 2.
A histogram-based calibration technique.

i th interval is

$$V_{r,i-1} \leq I_i \leq V_{r,i} \quad (1)$$

where $i = 1, 2, \dots, 2^n$, and the boundaries are given by $V_{r,0} = -V_R$ and $V_{r,2^n} = +V_R$ so that the ADC range is $2V_R$. In practice, these intervals are changed by offset errors, as in Fig. 1(b). In the case of large offset values, I_i may disappear, and another interval may be generated. In practice, many of the reference levels are displaced from their ideal locations, and combined with the comparator offset errors, these reference levels may overlap.

3 Calibration Technique

To calibrate the ADC, the error voltage sources, $V_{os,i}$ (Fig. 1), have to be estimated and compensated for. During estimation, the offset voltage or, as in many cases, just its polarity, is determined [3], [5], [6]. In trimming, the derived offset value can be compensated for by using analog circuit-level techniques.

In the proposed technique, estimation and trimming are performed without the comparator structure being modified. This ensures that the high-speed input signal is not adversely affected. Estimation can be performed without modifying the converter structure by relying on the input signal characteristics, as is commonly done in histogram-based test methods.

The basis of the proposed technique is shown in Fig. 2. The probability density functions (PDFs) of the input and output signals of the converter are

$f_{in}(x)$ and $f_{out}(x)$, respectively. The reference voltage of the ADC is V_R , and conversion is only valid for inputs in the range $-V_R < V_{in} < V_R$ because the ADC would otherwise saturate at either end.

An ADC system operates in normal or calibration mode. In normal mode, the input signal, V_{in} , is connected to the flash ADC input (node x in Fig. 2), and the ADC converts normally. In calibration mode, the output of the PDF generator is connected to the ADC input. The PDF generator produces an analog signal with a known probability density function, $f_{in}(x)$. The output PDF, $f_{out}(x)$, is a quantized version of $f_{in}(x)$. The output PDF is a discrete function in terms of I_i . The input PDF, however, is a continuous function. Because of static errors, the two PDFs are not equal. In histogram-based calibration, the difference between these two PDFs is used to extract the ADC errors.

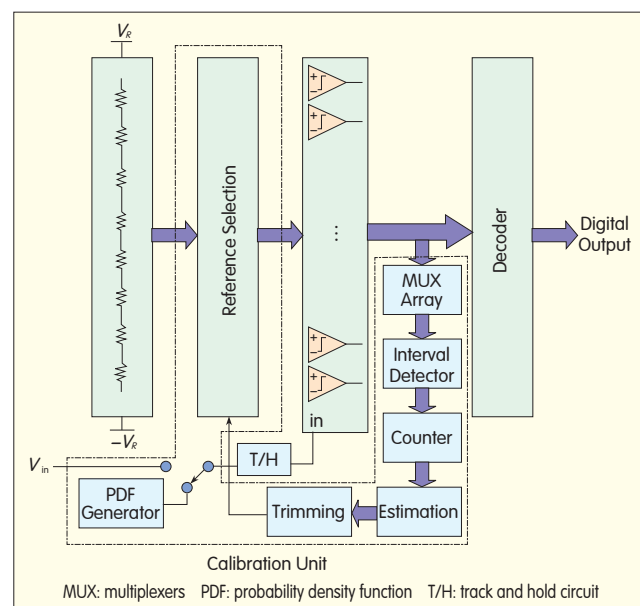
Fig. 3 shows an n -bit flash ADC that uses histogram-based calibration. The calibration units are indicated by the dashed line. An array of multiplexers (MUX) is used to select a set of comparators for calibration. The outputs of the array are connected to the interval detector block. This block determines which intervals, I_i ($i = 1, 2, \dots, 16$), the input

samples belong to. The counter records the number of samples for each interval. The ideal number of samples for each I_i is calculated because the input PDF must be known with reasonable accuracy.

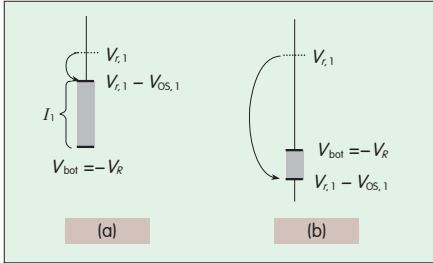
The estimation block estimates the error voltage source, $V_{os,i}$, by using the difference between N_i and N_i^* , where N_i is the desired number of samples belonging to I_i , and N_i^* (\sim denotes the non-ideal case) is the measured number of samples belonging to I_i . The estimations are then used by the trimming block to compensate for static errors. As described in section 5, this trimming block compensates for ADC error by adjusting the voltage taps of the resistor ladder. This adjustment changes the ADC reference levels, which are generated by the reference selection block.

4 Offset Error Estimation

For simplicity, the proposed calibration technique is used in a flash ADC with 16 decision levels, which corresponds to a resolution of $n = 4$ bits. The calibration technique is then extended to higher resolutions that have greater hardware complexity. In an IC implementation, extending the resolution limits the number of blocks,



▲ Figure 3. An n -bit flash converter. Additional calibration units are indicated by the dashed line.



▲ Figure 4. The effect of static error values on interval I_i for (a) small and (b) large errors.

(which grows exponentially with ADC resolution) so that the critical area does not increase too much.

4.1 Estimation for a Low-Resolution ADC

If the PDF circuit generates an analog signal with a uniform distribution (constant PDF) in the range $[-V_R, V_R]$, then for an ideal 4-bit converter, and for every sufficiently large batch of N input samples, on average

$$N_i = N/16 \quad (2)$$

samples in each interval $i = 1, 2, \dots, 16$. In a non-ideal 4-bit converter with interval I_i , as in Fig. 1(b), the expected number of samples is

$$\tilde{N}_i = \frac{2V_R - V_{os,i} + V_{os,i-1}}{2V_R} \times N. \quad (3)$$

By rearranging (3), a recursive expression is obtained:

$$V_{os,i} = V_{os,i-1} - 2V_R \cdot \frac{\tilde{N}_i - N_i}{N}. \quad (4)$$

Equation (4) can now be used to estimate the offset values, assuming $V_{os,0} = V_{os,16} = 0$. According to (4), comparators 1 and 15 give two initial estimated values:

$$V_{os,1} = -2V_R \cdot \left(\frac{\tilde{N}_1}{N} - \frac{1}{16} \right) \quad (5)$$

and

$$V_{os,15} = -2V_R \cdot \left(\frac{\tilde{N}_{16}}{N} - \frac{1}{16} \right). \quad (6)$$

Either one of (5) or (6) is a sufficient starting condition for the calibration algorithm. However, to minimize computational error accumulation during error estimation, the offset errors related to comparator 2 to 7 are

estimated using the initial condition (5), and offset errors related to comparators 8 to 14 are estimated using initial condition (6).

For large offset values, as shown in Fig. 1(c), I_i may disappear, creating a negative interval. In the case of an overlap, (4) must be modified so that the estimation can handle errors given by

$$V_{os,i} = V_{os,i-1} + 2V_R \cdot \frac{\tilde{N}_i + N_i}{N}. \quad (7)$$

This modified version of (4) is used instead of (4). The case of small offset values ($V_{os,i}$) in comparator 1 is shown in Fig. 4(a), where (5) is valid. For large error values, the reference level may be pushed below the bottom voltage $-V_R$, as in Fig. 4(b). In this case, $V_{os,1}$ is decreased during trimming until the situation shown in Fig. 4(a) is reached. Again, (5) is valid and can be used in the estimation process. The same strategy is used for the upper-end using a modified version of (6).

4.2 Extending to Higher Resolutions

To extend the low-resolution technique to a general n -bit converter, a segmented structure can be used (Fig. 5). This structure saves hardware for higher-resolution ADCs because a substantial part of the hardware grows linearly rather than exponentially. These benefits are described in more detail in [1].

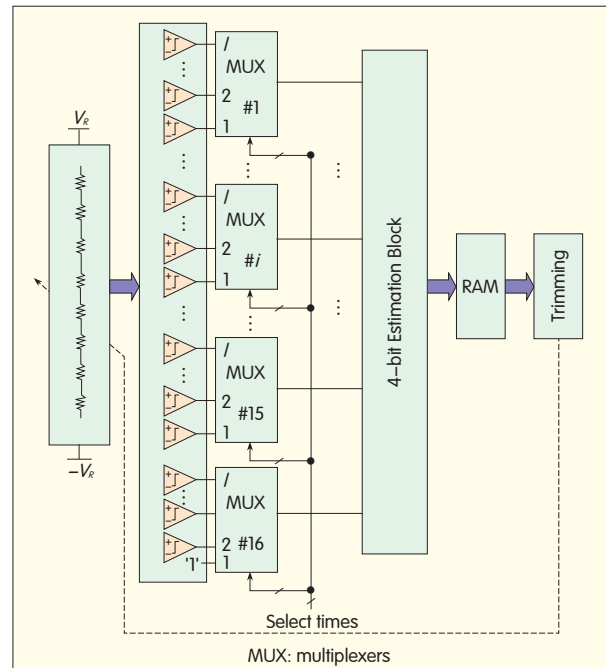
In the segmented approach, $m = 2^n - 1$ comparators are divided into $16 = 2^4$ subgroups (starting with the original 4-bits). Each group consists of $i = 2^{n-4}$ comparators, except for the last group, which contains $i - 1$ comparators. Sixteen multiplexers are used to choose the output of one comparator from each group and connect these to the 16-decision-level estimation block. At any

time during the calibration, 16 comparators are chosen and their offsets are estimated. The results are stored in a RAM. Then, another set of 16 comparators is selected for the estimation. This procedure continues until all offsets of all comparators have been estimated and stored in the RAM. Only one state, corresponding to a standard 4-bit flash ADC, contains $i - 1$ comparators. This is the state when the first input of each multiplexer is chosen.

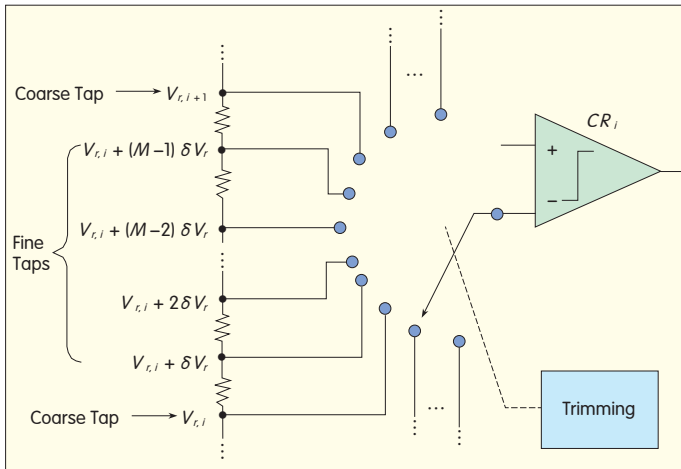
5 ADC Trimming Process

We take the trimming approach suggested by Chen et al. in [6]. Besides having single LSB steps for the ideal reference voltages, the resistor ladder also generates smaller steps, that is, fractions of an LSB to allow the reference voltages to be more finely adjusted. This implies that trimming is done without any changes being made to the comparator.

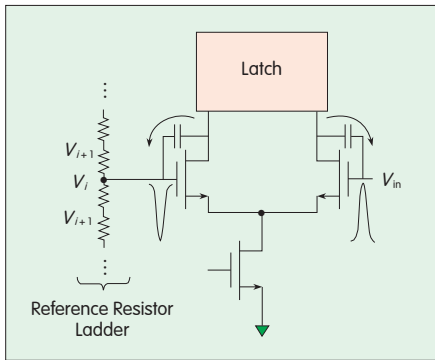
The approach is shown in Fig. 6. An appropriate voltage tap is selected by the trimming circuit in order to compensate for the offset value. In the resistor ladder, the coarse taps generate the ideal reference voltages,



▲ Figure 5. Extending 4-bit ADC calibration to an n -bit converter with $i = 2^{n-4}$ comparators in each group.



▲ Figure 6. Trimming a comparator by selecting taps from the resistor ladder.



▲ Figure 7. Kickback noise in a latched comparator.

$V_{r,i}$. In addition, there are M resistors between two consecutive coarse taps that generate $M - 1$ fine taps. Each fine tap generates a voltage of $V_{r,i} + \delta V_r$, where

$$\delta V_r = \frac{V_{r,i+1} - V_{r,i}}{M} \quad (8)$$

is the fine-level step — a fraction of the original coarse LSB step.

Our aim is to create a calibration process that does not adversely affect the performance of the ADC operating in normal mode. However, in practice, this is not possible. Any calibration changes or influences the ADC structure, and this can affect the overall performance.

Because more switches are added to the ADC's design (Fig. 6), kickback noise, a well-known problem, emerges. In a clocked comparator, the large variations on the regeneration nodes in the latch circuit are fed back through a

parasitic capacitor to the sensitive inputs of the comparator. This disturbs the input and reference voltages. A model of kickback noise is shown in Fig. 7 for an ordinary differential-pair comparator input stage.

To simulate the effects of kickback noise, a dynamic comparator with relatively large

kickback is chosen. This comparator is used in a 6-bit flash ADC architecture with a 0.5 V signal range, that is, $V_R = 0.25$ V. The number of sub-LSB steps is $M = 4$, see (8). The amplitude distribution for simulated kickback in different comparators is shown in Fig. 8.

The effect of the kickback noise depends on the reference level and the impedance of the resistor ladder at a particular node. If resistance between the taps of the ladder is very low, the kickback is very small. The noise amplitude is proportional to the impedance of each tap of the resistor ladder:

$$R_i = \left(i - \frac{i^2}{2^n} \right) \cdot R \quad (9)$$

where $i = 1, 2, \dots, 2^n - 1$ is the tap number, and R is the unit resistance of the reference ladder. According to (9), a symmetrical shape can be expected. However, the amount of kickback noise also depends on the input signal level as well as the reference level created by the voltage and capacitance differences between the gate and drain

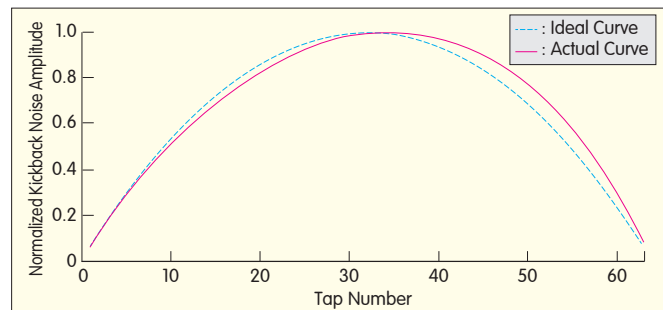
of input transistors. In particular, the values of the parasitic capacitors, C_{gs} and C_{gd} , change. Therefore, simulated noise is asymmetrical. In Fig. 8, we compare the normalized kickback noise levels for ideal and voltage-dependent cases.

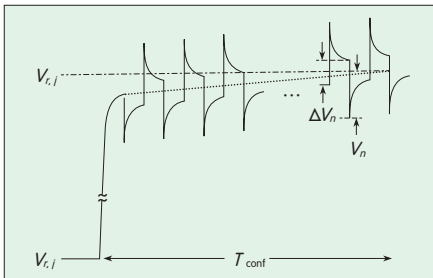
When extra switches are inserted for selecting finer reference levels, more decoupling capacitance is, by implication, added to different taps in the resistor ladder. Adding trimming circuitry does affect kickback noise but in a positive way.

An increased time constant is an important problem when the resistor ladder charges the comparator input. Using analog switches that are too small in order to save area makes the problem worse. However, the time constant appears as a configuration time, T_{conf} , which is the time the system takes to settle after the trimming command has been applied (Fig. 9). The perturbation is the effect of the kickback noise. The amplitude of the kickback noise is V_n , and the residual kickback error, caused by the resistor ladder's long settling time in response to kickback disturbance, is ΔV_n .

The additional analog switches are the configuration switches, and their on/off state is changed at the end of each calibration cycle. During the converter's normal operation, their state is fixed. Depending on the resistance of the resistor ladder and the size of the switches, the configuration time differs from a few clock cycles to several. The design of the circuits must include a time constant that is negligible compared with the overall calibration time. A more detailed picture of the effect of kickback noise on the calibration technique is given by the transistor-level simulation in [1]. The

Figure 8. ▶ Kickback noise for different tap numbers. The solid line represents the actual curve and the dotted line is the predicted curve when impedance variations are taken into account.





▲ Figure 9. Settling behavior of the resistor ladder in response to changing from reference level $V_{r,i}$ to $V_{r,i+1}$ (as a result of inserting a trimming command) also to kickback noise.

simulation uses a 65 nm CMOS with 1.2 V power supply.

6 Simulation Results

To determine the efficiency of the proposed calibration technique, a behavioral-level model of an 8-bit flash ADC using the segmented calibration technique was designed and simulated. A triangular signal generator (TSG) was used to realize a uniform distribution. The effects of an unwanted, non-uniform distribution caused by, for example, nonlinearity are discussed in [1]. The TSG, was configured so that a triangular waveform with a frequency of about 100 kHz was obtained, and the sampling frequency of the ADC was a modest 400 MHz.

The system design parameters and applied-error sources are shown in Table 1. Each calibration cycle contains the estimation of equivalent offset voltages for a set of 16 comparators chosen by the multiplexer array. In the case of interval overlap, one more calibration cycle is required. Further on, two calibration cycles are required to fully compensate for the TSG comparator offsets. Because an 8-bit converter is being studied, there are 16 sets of comparators to trim, and 64 cycles are needed to fully estimate and trim all the error sources in the ADC structure.

The estimation was implemented in register-transfer level (RTL) and synthesized on a Xilinx Spartan 3 FPGA. The post-synthesis code was used in the simulations, and 693 slices,

532 slice flip flops, and 1280 four-input lookup tables were also used.

One hundred Monte Carlo analyses were run, and the performance of the ADC before and after calibration was measured. The static performance in terms of DNL and INL is shown in Figs. 10(a) and (b), respectively. For about 98% of the Monte Carlo runs, the converter's performance considerably improved. After calibration, the DNL was reduced on average from 4 to 0.5 LSB, and the INL was reduced on average from 4.2 to 0.35 LSB. The failing 2% were cases where the offset was large enough to end up outside the correctable range.

7 Conclusions

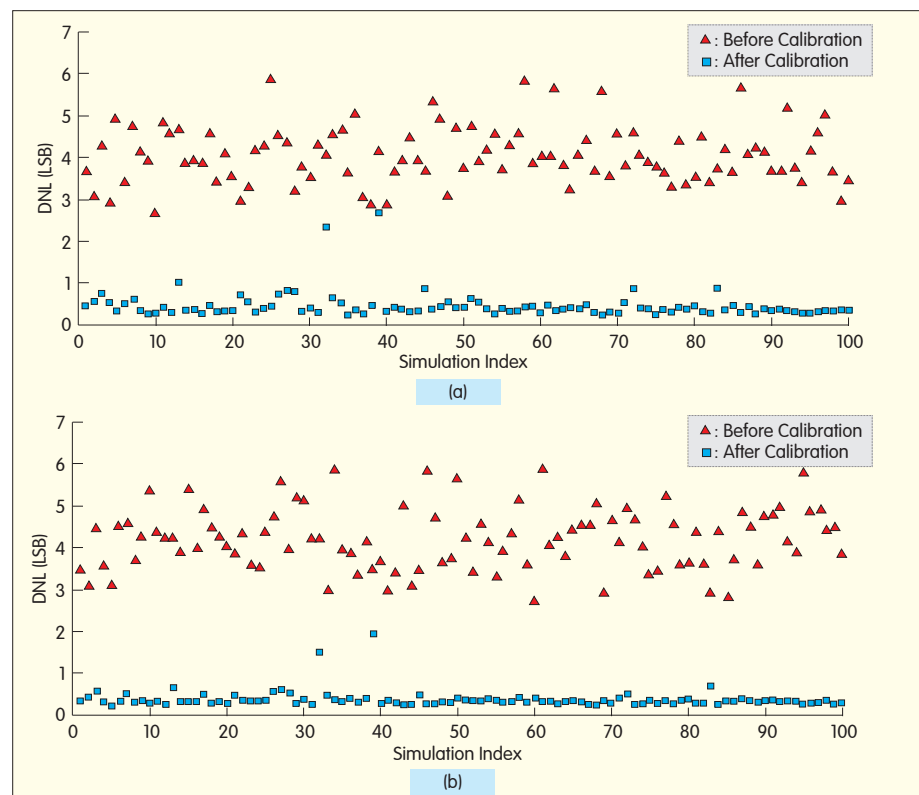
This paper describes a calibration technique for flash ADCs that is based on a histogram test method. The ADC is calibrated without its structure being adversely affected. Estimation is performed digitally,

and trimming is performed by adjusting the comparator reference voltages through arrays of analog switches.

A behavioral-level 8-bit flash ADC was designed, and typical errors were added to the comparators, resistor ladder, and PDF generator. The results of 100 Monte Carlo analysis show that converter performance was improved

▼ Table 1. Design parameters

Parameter	Value
ADC Resolution	8
Offset Distribution (σ_{os})	25 mV
Offset Distribution of TSG Comparators ($\sigma_{os,tsg}$)	5 mV
TSG Nonlinearity	5 %
Effective Resolution of Resistor Ladder	7 bits
Reference Voltage, V_R	1 V
Number of Samples Required in Each Calibration Cycle, N	2^{13}
Number of Calibration Cycles for a Complete Correction	64
Total Number of Samples per Calibration Instant	2^{19}
Number of Fine Voltage Steps, M	4
Word Length in Digital Part	12 bits
TSG: triangular signal generator	



▲ Figure 10. (a) DNL and (b) INL of the 8-bit flash ADC before and after calibration.

considerably in 98% of the runs.

This work can be used as a grounding for the study and implementation of ADC calibration techniques. Prospects and limitations of the technique are also highlighted in this work. An IC implementation of an ADC using the proposed calibration technique is detailed in [1].

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Biographies

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From P.34

elemental computing array (ECA), which is designed to achieve a better compromise between performance, flexibility, cost, and power efficiency. With ECA, the FGPA scheme can have performance, power, and cost similar to ASICs. ECA is far more flexible than a DSP with accelerators. It is also much cheaper and consumes far less power than FPGA devices.

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Biographies

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Advances in Mobile Data Communications



Sean Cai

Li Mo

This special issue of *ZTE Communications* focuses on recent advances in mobile data communications for the ICT and telecommunications industries. The ever-increasing amount of mobile data traffic has been the subject of many studies. This research area is widely applicable to contemporary technology and network optimization techniques.

The priority of most operators is to further expand their existing 3G networks and focus on new 3G technologies being developed to meet ever-increasing data traffic and data speed. Optimization techniques of 3G and 4G networks are being explored in order to improve network performance. Today, operators are concerned about adopting the right backhaul technologies, leveraging existing Wi-Fi networks to offload data traffic, building and evolving the core network, and introducing mobile cloud computing in order to support expanded business in the future.

In this special issue of *ZTE Communications*, we called for papers that provide greater insight into improved mobile data networks. Inter cell interference coordination (ICIC), coordinated multipoint transmission (CoMP), multiple input multiple output (MIMO), adaptive beamforming, and network load balancing (NLB) are introduced. These techniques may require operators to review the way they engineer and deploy their networks. Techniques to further improve network performance are discussed in this issue. High-level backhaul technologies and core network evolution paths are also discussed in this issue.

In “Enhanced Cell Edge Performance with Transmit Power Shaping and Multipoint/Multiflow Techniques,” by Philip Pietraski et al., a new concept called Fuzzy Cells is introduced to improve cell coverage. Fuzzy Cells enable user equipment (UE) to access the full system bandwidth in a sector by using a component carrier (CC) transmitted at higher power than the other CC frequencies. If at least three CC frequencies are used, three sets of cell boundary locations can be created so that no UE is simultaneously in the cell-edge region for every CC. Cell coverage can be improved using the techniques proposed in the article.

In “Spatial Load Balancing in Wide-Area Wireless Networks,” by Kambiz Azarian et al., NLB and single-carrier multilink (SCML) are compared. These techniques are used to increase network capacity and improve user experience. In NLB, each sector-carrier periodically provides its loading

information in order to improve overall network performance. In SCML, the combined burst rate of a UE can be significantly improved between neighboring cells.

In “Uplink Power Control for MIMO-OFDMA Cellular Systems,” by Rongzhen Yang, uplink power control algorithms, including FPC used in 3GPP LTE and LTE-Advanced, are compared. A novel power control algorithm is proposed for MIMO-OFDMA systems. A simplified maximum sector throughput (SMST) algorithm is also proposed to maximize the sector throughput by adjusting uplink transmit power.

In “Mobile Backhaul Solutions,” by Li Mo et al., mobile backhaul requirements are reviewed, and backhaul solutions are proposed with timing synchronization, multiprotocol label switching (MPLS); operation administration, and maintenance (OAM), and protection taken into consideration.

We thank all the authors for their excellent papers and the reviewers that had helped us with their careful and detailed critical reviews. We are very grateful to the editorial board for their helpful suggestions in improving the quality of the papers in this issue.

Biographies

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Enhanced Cell-Edge Performance with Transmit Power-Shaping and Multipoint, Multiflow Techniques

Philip Pietraski, Gregg Charlton, Rui Yang, and Carl Wang

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Abstract: In this paper, we present a technique called “fuzzy cells” that builds on the multicarrier features of Long Term Evolution-Advanced (LTE-A) and high-speed packet access (HSPA). Multiple carriers are aggregated to create a larger system bandwidth, and these carriers are transmitted at different powers by each sector antenna. This creates a set of cell-edge locations that differ from one frequency to the next. System-level simulations are performed to estimate individual user and average throughput for a hexagonal deployment of 3-sector base stations. For moderately high loads, a fuzzy cell deployment can improve tenth percentile (cell-edge) user throughput by 100% and can improve average throughput by about 30% compared with a reuse 1 scheme. Fuzzy cells reduce inter-cell interference in the same way as higher-order reuse schemes and allow users to access the full system bandwidth.

Keywords: LTE; fractional frequency reuse; multicarrier; flow aggregation; system simulation

1 Introduction

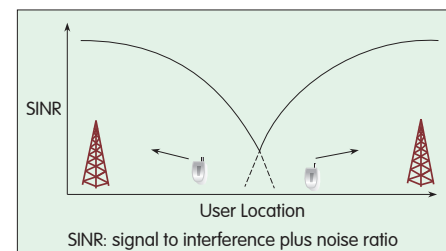
In current and evolving cellular systems (LTE is the example in this paper) [1], it is generally very difficult to create a uniform user experience because throughput at the cell edge is limited by interference from other cells. In standard frequency reuse 1, the cell-edge downlink (DL) signal to interference plus noise ratio (SINR) can be less than 0 dB, which limits user throughput even if there is a large number of resource blocks (RBs) for UEs. The cell-edge problem is shown in Fig. 1.

For UEs close to an E-UTRAN Node B (eNB), the DL SINR is quite high. However, as the UE moves away from the eNB, the DL SINR decreases until the UE is midway between the eNBs (at the cell edge). A handover (HO) then occurs; the UE passes to the next eNB, and SINR starts to increase again. SINR is lowest near the cell edge. In a typical two-dimensional

hexagonal deployment, this cell-edge condition affects much of the deployment area. In an OFDM system, such as LTE Release 8, the cell-edge problem can be mitigated to some extent by organizing UEs into groups according to different parts of the spectrum and using different transmit powers for these groups.

Cell-edge UEs are grouped logically. They are assigned a specific part of the spectrum and are allocated a potentially higher power, as in soft frequency reuse (SFR), or higher frequency reuse transmission, as in fractional frequency reuse (FFR). Although the data signal received by cell-edge UEs may be improved, this approach has limitations. Take, for example, the cell coverage and control channel. The control channel spans the system bandwidth and is shared among UEs. Thus, the same extended range that a frequency selective, UE-specific data channel might attain is not possible for UEs at the cell edge.

More importantly, some UEs will not have access to the full system bandwidth. In the FFR case shown in Fig. 2, the spectrum is split into two parts: reuse 3 and reuse 1. Some of the UEs are classified as cell edge, and others are classified as cell center. The classification determines which parts of the spectrum are available to the UEs. The details depend on the particular FFR scheme, but the cell-edge UEs are expected to have improved SINR in the red, blue, or green frequency areas. Improved SINR comes at the price of reduced accessible bandwidth for UEs.



▲ Figure 1. Cell edge in a one-dimensional deployment.

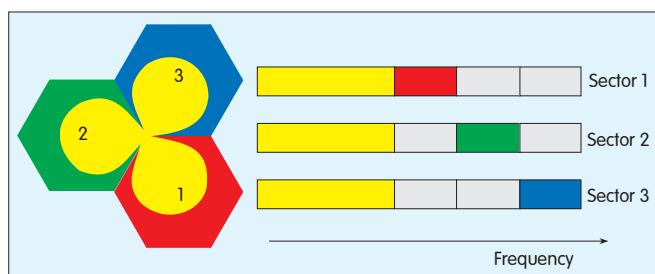


Figure 2.
FFR spectrum distribution.

In LTE Release 10, carrier aggregation (CA) of component carriers (CC) allows spectrum to be aggregated. Each CC has a bandwidth that is compatible with Release 8, but UEs can attach to and be scheduled on multiple CCs. Each of these CCs can be considered a cell of its own with a different carrier frequency and, potentially, different coverage areas. Differences in coverage may occur as a result of differences in propagation conditions; however, system transmit power, HO thresholds (for example, cell biasing), and even sector antenna direction can be changed to modify the DL coverage. This solves the control channel problem; the power of the control channel can be adjusted for each CC, thus enabling SFR. However, the problem remains that UEs cannot access the full system bandwidth.

The cell-edge problem in Fig. 1 has also been approached from the perspective of intercell interference (ICI) and ICI mitigation using coordinated base stations [2]. Adjacent cooperative base station clusters can generate different interference levels in different frequency subchannels by optimizing power allocation to those subchannels. In this way, SINR near the cluster edge can be improved without the need for fast coordination between the clusters. In [3], this approach was analyzed in a one-dimensional space, and power allocation was optimized based on an SINR balancing condition at fixed locations in the cluster. Therefore, power allocation depended only on the system's geometry, and the effects of adjusting the transmit power on cell loading were not taken into account. The fuzzy cells technique relies on system capabilities that enable transmitting multiple powers on different carriers and transmitting data

to UEs from different base stations on different CCs.

2 Fuzzy Cells

2.1 Definitions

Sector antenna: an antenna that provides coverage to an area in one or more of the CC frequencies that make up the system bandwidth. In the examples discussed herein, sector antennas support either three or six CC frequencies.

Site: a collection of co-located sector antennas. Each site is composed of three sector antennas, and all sector antennas at a site are part of the same eNB.

Hexagon: a geographical area defined by site locations only. A hexagon is defined by geometry and is not affected by transmit antenna power and shadowing.

CC frequency: a frequency band carrying the data and control signals of a particular CC. The sum of all the CC frequencies is the total system bandwidth.

CC: is a component carrier in an aggregation of carriers. This comprises the CC frequency and sector antenna.

Its coverage area is determined by UE-CC selection rules and parameters, for example, transmit power and cell bias. It is close to the usual definition of a cell or sector.

Cell edge UEs: the set of UEs in which throughput levels are at most those represented by the tenth percentile of UE throughputs.

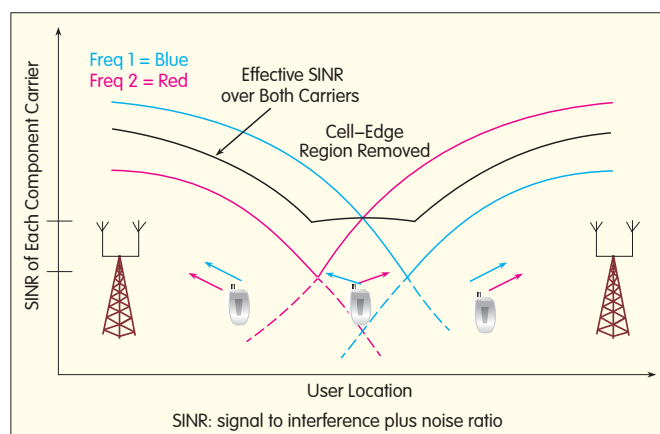
UE perceived throughput: the number of bits downloaded by a UE divided by the time that the UE has data in its buffer to be transmitted.

2.2 Fuzzy Cell Concept

The key to fuzzy cells is enabling a UE to connect to the best CC in each CC frequency regardless of the site in which the CC originates. Enabling the UE to connect in this way allows a UE to access the full system bandwidth when SFR-type power allocation is used. Then, a good SINR can be achieved in each CC frequency within the system bandwidth. Multisite connection is shown in Fig. 3. As the UE crosses the cell boundary in a given CC frequency, it drops that CC and picks up a new CC from a different site in the same CC frequency. In this way, the UE always has access to full system bandwidth even midway between sites. The cell edge is blurred, creating the concept of a "fuzzy" cell. The resulting cell-edge performance is enhanced, and this improvement can be measured in terms of equivalent SINR (eSINR).

Equivalent SINR is the SINR needed to maintain the same throughput over the entire system bandwidth (assuming the same SINR is observed over the entire system bandwidth). To calculate

Figure 3. ▶
Cell-edge improvement
in one-dimensional
fuzzy cell.



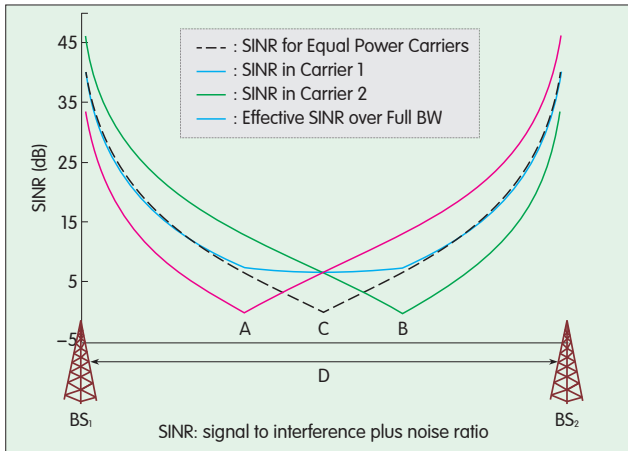


Figure 4. eSINR for two isolated base stations.

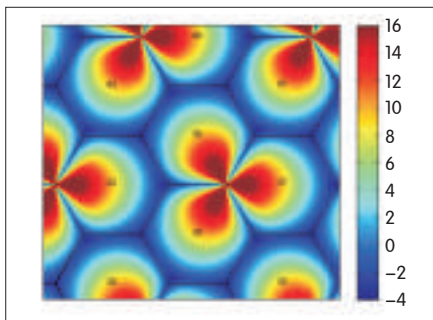


Figure 5. Two-dimensional color map of SINR for reuse 1 baseline.

eSINR, first, the SINR for the UE in each CC with which it is associated is determined. The SINR for each of these CCs is then mapped into an achievable throughput using the Shannon Capacity formula. The achievable throughput in each CC is summed, and the result is mapped back into the eSINR, given by

$$eSINR = 2^{\sum_{n=1}^N \log_2(1 + SINR_n)/N} - 1 \quad (1)$$

where n is the index of the CC, N is the number of CC frequencies, and $SINR_n$ is the SINR of the UE in CC frequency n . Fig. 4 shows SINR and eSINR in the case of two isolated base stations, each with two CCs transmitted with a power difference of 12 dB.

The red and green curves represent SINR for CC frequency 1 and CC frequency 2, respectively. The black curve is the eSINR when the transmit powers of both frequencies and base stations are identical. The blue curve is the improved eSINR resulting from different transmit powers at the base stations. Cell-edge eSINR is improved by multisite connections and different

coverage areas for the two CC frequencies.

2.3 Fuzzy Cell SINR in a Two-Dimensional Deployment

Fig. 5 shows a two-dimensional plot of SINR for a typical hexagonal site with three sectors per site. With reuse 1, each cell has a coverage area that approximates the shape of a hexagon. Assuming the eNB transmit powers are sufficiently large to limit system interference, the worst possible SINR is less than -4 dB without shadowing (Fig. 5). With shadowing, the SINR may be even lower. This scenario is used as a baseline case.

2.4 eSINR in a Fuzzy Cell Deployment

Unlike the cell boundaries in the reuse 1 baseline (Fig. 5), cell boundaries in a fuzzy cell deployment are no longer hexagonal (Fig. 6). In the first CC frequency, applying higher transmit powers from some sectors creates larger cells. In another CC frequency, the same phenomenon occurs, but the pattern is rotated. If at least three CC frequencies are used, three sets of cell boundary locations are

created so that no UE is simultaneously in the cell-edge region for every CC. The cell boundaries are moved by changing the transmit power and by moving from one CC frequency to the next. In Fig. 6, ΔP between high and low power transmitters is 12 dB. The magenta contours delineate where $SINR = 0$ dB and are an estimate of the cell boundaries.

In Fig. 7, the eSINR of the fuzzy cell deployment is shown alongside that of the baseline. Although the maximum eSINR is lower in the fuzzy cells than in the baseline, there is no place in the fuzzy cells where eSINR drops below 0. This shows that fuzzy cell configuration better services cell-edge users. The cumulative distribution functions (CDFs) for eSINR in fuzzy cells and baseline (Fig. 8) show that eSINR at the 10th percentile is improved by approximately 4 dB when using a fuzzy cell configuration.

2.5 UE-CC Association Strategy

Every UE can be associated with the sector antenna in each frequency that provides the best biased SINR. Biasing artificially extends the coverage area of small cells or is used for load balancing. With a small bias, ICI is limited because the cell boundary is only slightly extended. However, more users are associated with CCs transmitted at high power, and this decreases the resources available to each user in those CCs. Conversely, a large bias better balances the resources available to each user at the expense of smaller SINR improvement. A tradeoff is necessary to obtain the best combination of cell-edge and overall average throughput. Ideally, cell-edge throughput is significantly improved at the cost of a modest

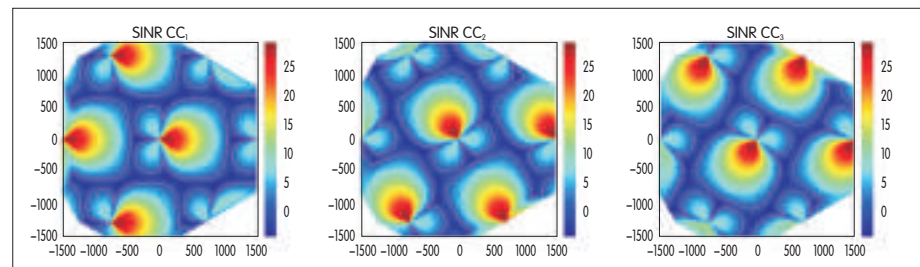


Figure 6. Two-dimensional SINR for a fuzzy cell deployment.

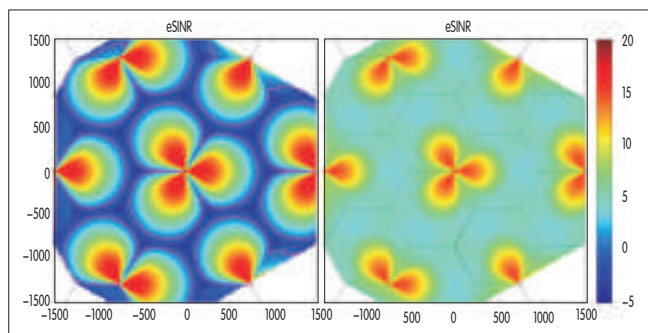


Figure 7. Two-dimensional SINR for baseline (left) and eSINR for fuzzy cells (right).

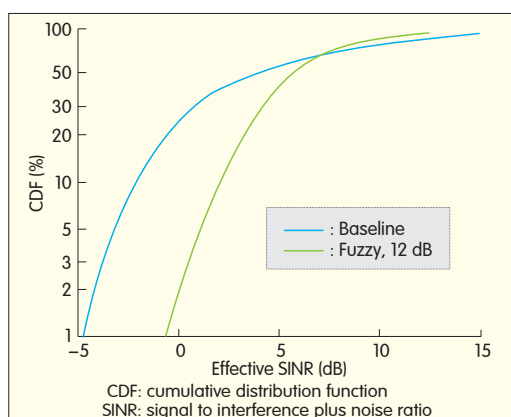


Figure 8. CDF of eSINR of fuzzy cells and baseline.

reduction in overall throughput. However, for cells that are realistically loaded, it is possible to improve both cell-edge and average throughput. The CCs providing the largest-biased SINRs in each frequency are assigned to each UE. The bias applied to the SINR involves optimizing one of the system parameters so that the tenth percentile user throughput is maximized for each average throughput value.

2.6 Impact of Backhaul Data Flow Split on Performance

Fig. 9 shows the splitting of the downlink data flow in a fuzzy cell deployment. The split occurs in the eNB. The application data packet is downloaded from the core network to the serving eNB (eNB1) via S1 interface. The eNB1 decides how to split received data for each UE, and the data payload is split in two. Part 1 is sent to the UE directly from the eNB1, and part 2 is forwarded to the cooperating eNB (eNB2) via X2 interface before being sent to the UE by the eNB2. Status signals are frequently

sent over the backhaul to control data-flow splitting.

X2 latency modifies the start and end times of the period where fuzzy cell operation produces gains. When the application packet arrives at eNB1, data is immediately transmitted to the UE but only from eNB1. Fuzzy cell operation begins only after the initial X2 data forwarding delay to eNB2; that is fuzzy cell gains are only possible when both eNBs have data to send. Similarly, if one of the eNBs empties its buffer for the UE before the other eNB, then the fuzzy cell gains are also lost. If eNB1 finishes transmitting part 1 before eNB2 finishes transmitting part 2, then at that point, only eNB 2 can transmit to the eUE.

The packet size for the traffic model in [2] is 2 MB. For a 2 MB packet and an assumed X2 delay of 10–20 ms, the delay is negligible and not modeled in the simulations.

2.7 Estimating Performance

Because of the complexity of cellular systems, it is difficult to predict gains without extensive simulation; however, some estimation is possible. For lightly loaded cells, UEs do not contend much for resources in any given transmission time interval (TTI). In this case, the throughput distribution can be largely predicted by the eSINR distribution, and the eSINR can be mapped to an achievable throughput. If we consider only the long-term SINR in each CC frequency in the system, we can compute the achievable

throughput for each UE in the system using all its connected CCs. The long-term SINR can be used as a rough estimate of throughput in a fading environment. Fig. 10 shows achievable throughput distribution for a power difference of 10 dB. From this graph, we can expect cell-edge throughput to be nearly 85% better than in the baseline and still have similar average UE throughput. Furthermore, if two of the three CCs are switched off at each sector antenna (indicated by a power difference of 100 dB in Fig. 10), eSINR distribution is further improved. The tenth percentile throughput is nearly 160% better than in the baseline, and there is nearly 30% increase in average UE throughput. This estimate is only accurate if there is little or no competition among UEs for radio resources. As the loads increase towards full buffer-like operation, the load imbalance between large- and small-coverage area CCs has a greater impact on performance, and

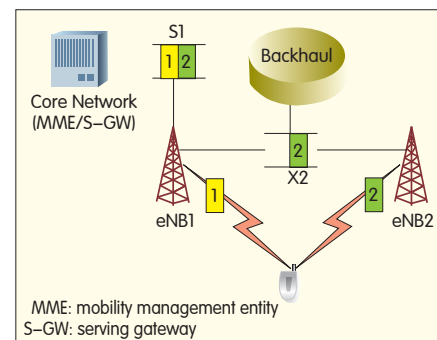


Figure 9. Data-flow splitting at eNB.

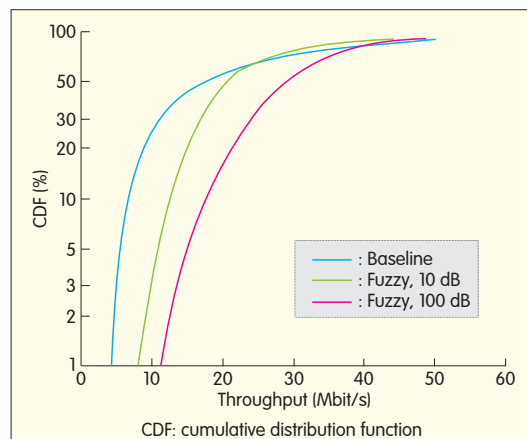
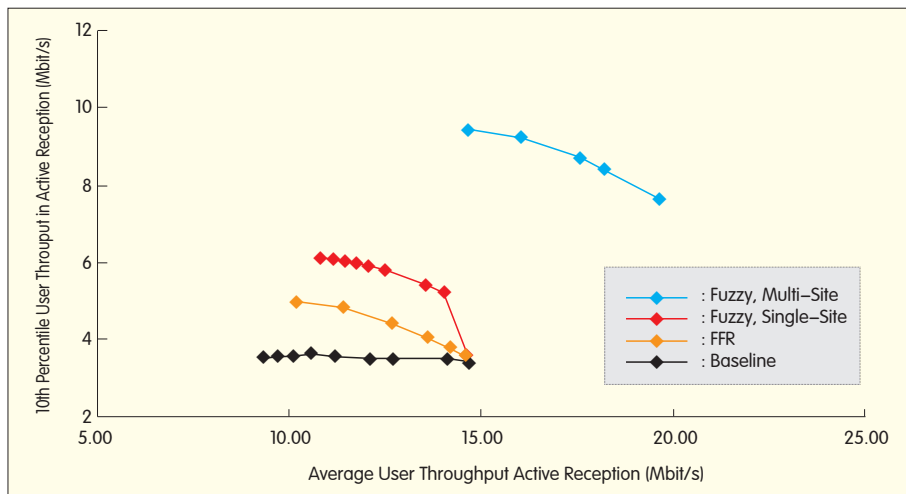


Figure 10. eSINR based achievable throughput CDF for a 10 dB power difference.



▲ Figure 11. Comparison of algorithmic schemes for high traffic with shadowing.

eSINR alone cannot be used for estimation. In other words, improving the SINR in some CCs by increasing transmit power must be weighed against the increased load these CCs will have because of their larger coverage areas. It is not clear what the optimum tradeoff is, and we must rely on simulations to provide performance estimates. Smaller power differences are also preferable as the traffic load increases.

Even in a heavily loaded system, that is, 50% resource use, there are many TTIs where a UE has little competition for resources in a given CC. Consequently, there are some TTIs in which the eSINR is a predictor of performance.

3 Simulation Results

Throughput based simulations were carried out to compare the performance of different types of fuzzy cell deployments to the performance of the baseline case and FFR schemes. We consider two main metrics of importance: average UE perceived throughput and the cell edge UE-perceived throughput. Because there are two metrics of interest, it is instructive to present data as the possible tradeoff between them. There is tradeoff between average UE-perceived throughput and the cell-edge UE-perceived throughput. For example, even in the simple

baseline case with PF scheduler, a tradeoff between cell-edge and average throughput can be achieved by varying the fairness exponent (β) in the scheduler. By sweeping β , we generate the parametric curve of cell-edge user throughput versus average throughput. There are several parameters that affect the performance of FFR and fuzzy cell cases. To obtain the tradeoff curves, optimizations were performed to find system parameters that maximized the tenth percentile throughput subject to different average throughput constraints. The other parameters optimized were the cell biasing and the difference in power between the high tx power CC and the two lower-power CCs on each sector antenna. Similar optimizations are done for the parameters that describe the FFR and SFR techniques.

3.1 High-Volume Traffic

Here, a comparison of fuzzy, FFR, and baseline schemes for high-volume, bursty traffic is discussed. High-volume traffic means the traffic load corresponds to RU of about 50% in the baseline scenario. Two types of fuzzy results are shown in Fig. 11: multisite fuzzy and single-site fuzzy. The former are results from simulation of multiflow data delivery scheduling on the best CC regardless of the site at which the CC originated. This is the same fuzzy cell scenario previously described. The latter are

results from simulation of multiflow data delivery scheduling restricted to CCs originating from the same site. This is more compatible with LTE-A Release 10.

Multisite fuzzy cells double edge-user throughput and improve average user throughput by roughly 30% compared with FFR and baseline schemes.

3.2 Low-Volume Traffic

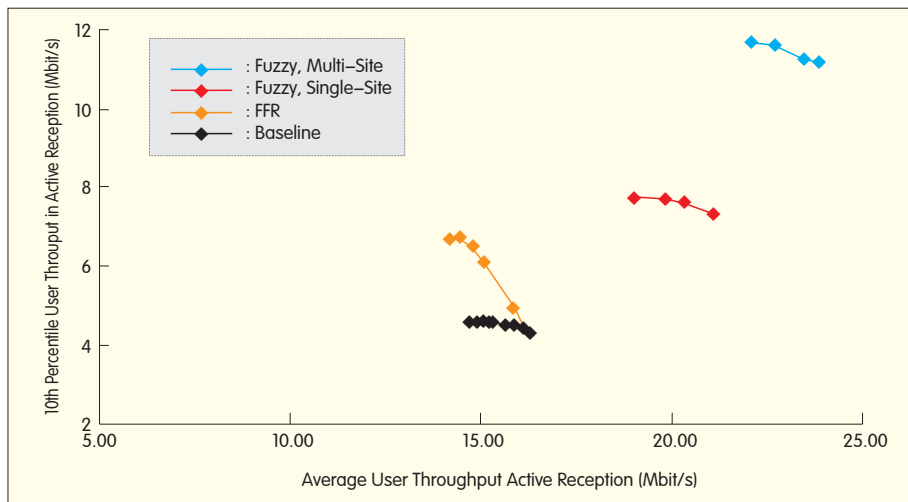
Here, a comparison of fuzzy, FFR, and baseline schemes for low-volume, bursty traffic is discussed. Low-volume traffic implies an RU of about 10% in the baseline case. Similar to the high volume traffic case, low volume traffic fuzzy results are shown in Fig. 12. Multisite fuzzy doubles improvement in edge-user throughput and improves average user throughput by roughly 60% compared with FFR and baseline schemes.

4 Conclusions

Fuzzy cell technology combines multipoint, multifrequency transmission techniques, and intelligent parameter selection (e.g. transmission power differences between carriers), and it is built on top of carrier aggregation. It can be applied to any multicarrier system, including HSPA+ and LTE.

Fuzzy cells is a simple, high-performance, robust scheme that mitigates the cell-edge problem and improves system performance. We have shown the cell edge versus average performances that can be achieved with standard frequency reuse 1, FFR, and fuzzy cells. Fuzzy cells roughly doubles cell-edge performance compared with frequency reuse 1 and FFR. Fuzzy cells also significantly improve average performance.

In fuzzy cells, the data flow to each UE in a CC is independent in terms of radio resource scheduling and hybrid automatic repeat request (HARQ). Therefore, allocations among different sites do not need to be tightly coordinated. The need for stringent latency is relaxed compared with CoMP inter-site coordination via the X2 interface. To support techniques such



▲ Figure 12. Comparison of algorithmic schemes for low traffic with shadowing.

as CoMP, investment needs to be made in low-latency, high-capacity backhaul, for example, fiber optics. However, fuzzy cells can be realized with existing backhaul. Fuzzy cells can be realized before other advanced techniques and without investment in new low-latency backhaul.

Appendix

A system-level simulator using hexagonal cellular layout is used to validate our concept. The simulation parameters are based on LTE urban

macro cell no line-of-sight. UEs are dropped randomly with uniform distribution. The simulation parameters are summarized in Table 1. Two site rings are populated with users, and statistics are collected only from UEs near the center site.

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▼ Table 1. System simulation parameters

Carrier Frequency	2 GHz
Bandwidth per CC	3 MHz
Number of CC frequencies	6 or 3 (6 CCs are used for comparison with FFR techniques and to allow the system bandwidth to be split into reuse 1 and reuse 3)
Number of Antennas per Link	1 Tx, 1 Rx
Average CC Transmit Power	41 dBm
Number of RBs per CC	15
Number of Sector Antennas per Site	3
Inter-Site Distance (ISD)	500 m
Total Number of Sites	19
Number of UEs per Site	30 (10 per Sector Antenna)
UE Distribution	Uniform Distribution Random Drop
Channel Model	—
Path Loss	$PL = 161.04 - 7.1 \log_{10}(W) + 7.5 \log_{10}(h) - [24.37 - 3.7(h/h_{bs})^2] \log_{10}(h_{bs}) + [43.42 - 3.1 \log_{10}(h_{bs})] [\log_{10}(d) - 3] + 20 \log_{10}(f_c) - \{3.2 [(\log_{10}(11.75 h_{ur}))^2 - 4.97]$
Street Width (W)	20 m
Avg. Building Height (h)	20
h_{bs}	25
h_{ur}	1.5 m
Shadow Fading	—
Shadowing Standard Deviation (σ)	6 dB
Correlation Dist (dcor)	50 m
Multipath Channel	EVA 30 kph
UE thermal Noise Density	-174 dBm / Hz
Noise Figure	7 dB
TTI Length	1 ms
Sector Antenna Parameters	—
Antenna Pattern	$A(\theta) = -\min[12(\theta/\theta_{3dB})^2, A_m]$
Peak Antenna Gain	14 dBi
3 dB Beamwidth (θ_{3dB})	3 dB @ ± 70 Degree
Front/Back Ratio (A_m)	20 dB
Scheduler	Proportional Fair. Common Pool Buffer. Perfect CSI Information. 1 RB Granularity.
Beta	Optimized in Simulation
Link Performance Model	EESM
Interference Model	AWGN with Power Based on PL and per CC Tx Power Setting
X2 Latency	0 ms
Traffic Model	3GPP FTP Model 1
Packet Size (S)	1 MB
User Arrival Rate (λ)	0.00063 (high load) or 0.00013 (low load) Packets/TTI/UE Corresponds to Approximately 50% and 10% Resource Utilization
Simulation Duration	50 s/drop

Biographies

Phil Pietraski (philip.pietraski@interdigital.com) received his BSEET degree from De Vry University in 1987. He received his BSEE, MSEE, and Ph.D. degrees from Polytechnic University, Brooklyn, NY in 1994, 1995, and 2000. He also has a graduate certificate in wireless communications from Polytechnic University and studied accelerator physics at the U.S. Particle Accelerator School (hosted by universities including Harvard and Duke). He joined InterDigital Communications in 2001 and is currently a principal engineer who leads research in wireless communications. He holds more than 30 patents in the field. Prior to his transition to communications in 2000, he was a research engineer at Brookhaven National Laboratory, National Synchrotron Light Source, responsible for developing spectroscopic and imaging, solid-state and gaseous, X-ray detectors. He has also conducted research at the Polytechnic University for the Office of Naval Research (ONR) in underwater source localization using passive SONAR.

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Spatial Load Balancing in Wide-Area Wireless Networks

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Abstract: Load balancing is typically used in the frequency domain of cellular wireless networks to balance paging, access, and traffic load across the available bandwidth. In this paper, we extend load balancing into the spatial domain, and we develop two approaches—network load balancing and single-carrier multilink—for spatial load balancing. Although these techniques are mostly applied to cellular wireless networks and Wi-Fi networks, we show how they can be applied to EV-DO, a 3G cellular data network. When a device has more than one candidate server, these techniques can be used to determine the quality of the channel between a server and the device and to determine the load on each server. The proposed techniques leverage the advantages of existing EV-DO network architecture and are fully backward compatible. Network operators can substantially increase network capacity and improve user experience by using these techniques. Combining load balancing in the frequency and spatial domains improves connectivity within a network and allows resources to be optimally allocated according to the p-fair criterion. Combined load balancing further improves performance.

Keywords: CDMA 2000; EV-DO; DO-RevC; high rate packet data (HRPD); network load balancing (NLB); single-carrier multilink (SCML)

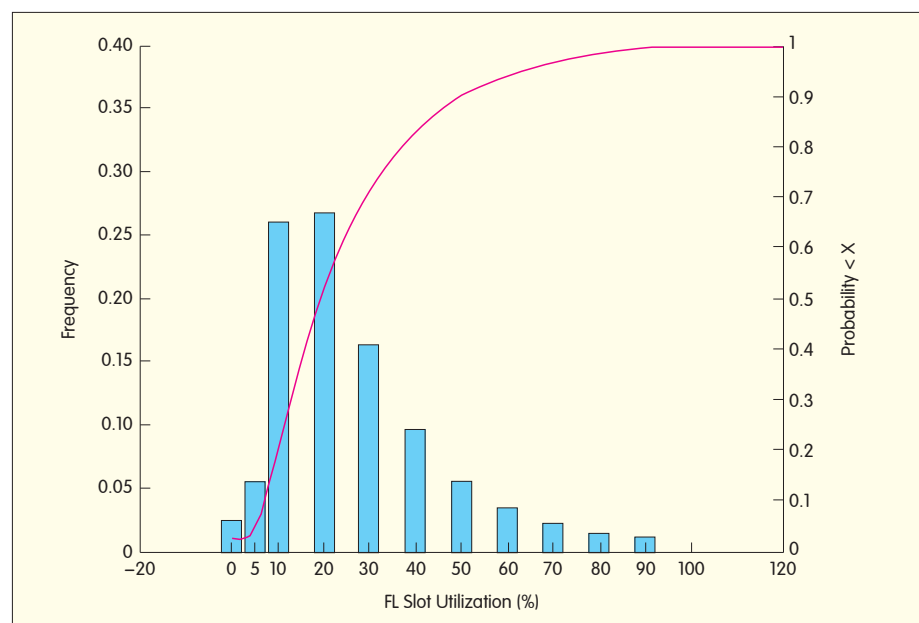
1 Introduction

Demand for data in wireless networks is spatially non-uniform, which leads to chokepoint sectors, and it is also time-varying, which means that chokepoint sector locations change. Chokepoint sectors operate at or close to the maximum load; therefore, they determine network performance, user perception of network performance and, ultimately, user experience. In a network with fixed assets and unbalanced loading, spatial load balancing uses network resources from neighbors of chokepoint sectors to serve users in the chokepoint sector. This increases the capacity of the network.

Field data collected from commercially deployed networks shows that only a small fraction of sectors are chokepoints at any given time and that chokepoint sectors typically have several lightly loaded neighbor sectors. Fig. 1 shows the distribution of sector

loading (per-sector forward link (FL) slot use) during peak hour in a metropolitan commercial EV-DO network where sectors with low slot use

are lightly loaded. Operators add hardware by splitting cells near the chokepoint sectors or increase bandwidth by adding carriers to the



▲ Figure 1. Per-sector FL slot use during peak hour (mean FL use is 26%).

chokepoint sectors. Such actions lead to networks that are designed for worst-case scenarios and are therefore underused most of the time.

The spatial load-balancing techniques discussed in this paper are network load balancing (NLB) and single-carrier multilink (SCML).

In NLB, a device is opportunistically reassigned from a heavily loaded sector to a lightly loaded sector, even if the channel quality of the heavily loaded sector is better. The end result is increased capacity for the chokepoint sector from offloading the most expensive users (poor channel quality means that the network has to allocate more resources for a given amount of traffic) to the neighbor sector.

With SCML, any device that can simultaneously process two or more independent data streams can achieve the benefits of a multicarrier network, even though the device may be in the hand-off region of a single-carrier deployment.

With multicarrier EV-DO, the EV-DO carriers that serve a mobile device use different carrier frequencies and may originate from the same cell or different cells. With SCML, the same carrier frequency serves the mobile device with independent data streams and from different sectors. NLB improves performance when the chokepoint sector is loaded, and SCML improves performance at all load levels. In this paper, we describe how these techniques augment load-balancing in the frequency domain.

In Section 2, we provide necessary background information. In sections 3 and 4, we discuss the concepts, algorithms, and implementations of NLB and SCML. In section 5, we perform simulations to determine the performance of NLB and SCML. In section 6, we make concluding remarks and discuss future work.

2 Background

2.1 Server Selection

When the access terminal (AT) in a wireless network has a choice of serving sectors, it typically selects the

server with the best channel quality. (Here, hysteresis based on channel quality and time is not discussed for the sake of simplicity.) In EV-DO, the AT selects the best forward layer (FL) server from the candidate servers that have a corresponding reverse link (RL) of acceptable quality. If the DRCLock bit on, the RL quality is acceptable; if the DRCLock bit is off, the RL quality is unacceptable. The DRCLock bit itself is set according to the quality of the RL overhead channels received at the base station.

2.2 Multicarrier Operation

When an AT in EV-DO is assigned multiple carriers, those carriers may originate from the same sector or different sectors (one forward-link serving sector for each carrier) [1], [2]. Commercial EV-DO uses independent schedulers on each sector carrier, and multicarrier EV-DO uses multilink radio link protocol (RLP) on each sector carrier. Multilink RLP enables the network to split a data stream at the transmitter across multiple independent schedulers and to combine the data stream at the receiver while ensuring early detection of packet loss and in-order delivery of RLP packets [3]. When multiple links (or carriers) are assigned to an AT, the network distributes forward-link data across available links. Data throughput on each link can be different, and the throughput varies over time. Enhanced flow control (EFC) ensures FL data is distributed across links according to link throughput and that the data distribution adapts to changes in link throughputs.

Each forward link in EV-DO requires reverse-link feedback to indicate FL channel quality and acknowledgements (ACK/NACK) for physical-layer HARQ. EV-DO supports multiple feedback multiplexing modes. RL overhead of multiple FL carriers can be transmitted over a single RL carrier to minimize the RL pilot overhead.

2.3 FL Load Metrics

We introduce a new metric for the loading at each sector. This metric is the average number of non-empty

queues at the sector carrier. It is calculated for each slot (which takes 1.66 ms) and is fed to a filter with a time-constant of a few seconds to generate the Neff metric.

Networks are at times backhaul-limited, and this leads to the air link at the BTS being underused. A backhaul-limited sector-carrier may not appear to be loaded because of queue under-run. Therefore, backhaul limit must be accounted for when calculating loading level at each sector-carrier. A metric for backhaul limit is the number of unfilled flow control requests for a sector-carrier that has non-empty AT queues at the BSC.

2.4 Operator Deployments

Operators deploy wireless data networks according to data demand. Hence, operator deployments are not uniform and have spatial variations in the number of carriers deployed. Typically, a large area in an operator network has three or less deployed carriers. In regions of the network with just one carrier, multicarrier EV-DO cannot improve performance of ATs with multicarrier capability.

2.5 Smart Carrier Management

EV-DO access networks (ANs) assign the best-available carrier to an AT by transporting the load levels across carriers (on the forward and reverse links) and the channel quality from the ATs to each of the candidate carriers.

3 Network Load Balancing

NLB is shown in Fig. 2. PN (b) is the best FL sector for the user; however, PN (b) is heavily loaded and the neighboring sector, PN (a), is lightly loaded. If PN (b) is selected as the serving sector, it has better signal-to-interference plus noise ratio (SINR) than PN (a) but is scheduled much less time than in PN (a) because of heavy loading. Thus, even at the cost of FL SINR degradation, the AT's throughput can increase when the FL loading differential is sufficient to offset the SINR degradation.

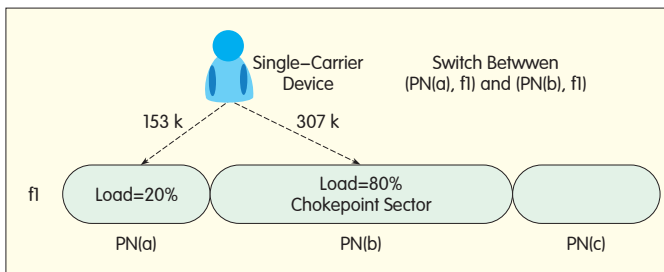


Figure 2.
Network load balancing.

An important consideration in NLB is its interaction with the partial loading of neighboring sectors. The SINR of the traffic channel in the chokepoint sector is higher than the SINR of the pilot channel (only applicable to EV-DO) because of lesser interference from the lightly loaded neighboring sector. If the AT is served by the lightly loaded neighbor, then the chokepoint sector with high neighbor loading gives strong interference. If a network has a large number of ATs with the ability to spatially null the strong interferer, the network can gain more from NLB. In addition, offloading users to lightly loaded neighboring sectors drives those sectors towards higher slot use, and these sectors then cause more interference to the chokepoint sector. This effect limits the loading differential across sectors where NLB is beneficial. The NLB algorithms also specify minimum FL channel quality to ensure the AT does not choose an extremely weak FL server, regardless of the load difference between neighboring sectors. This allows the AT to continue to receive the FL control channels with the desired performance. There are two types of NLB algorithm: one for existing ATs deployed by operators and another for new ATs.

3.1 Network Load Balancing for Legacy ATs

Implementation of the NLB algorithm for legacy ATs does not require the AT to have any additional capability. Each sector-carrier periodically provides its load information (Neff) to the BSC. The BSC also receives FL pilot strength information from ATs via a RouteUpdateRequest in EV-DO every 2 to 4 seconds. With this information, the BSC can select suitable legacy ATs and induce them to change serving

sectors by setting the DRCLock bit (RL quality indicator) that corresponds to the chokepoint sector to off (indicating poor RL quality).

3.2 Network Load Balancing for New ATs

The AN assists NLB for new ATs. Each sector-carrier periodically provides its Neff to the BSC. The BSC propagates this to all members in the neighbor list of each sector-carrier. Each sector-carrier periodically broadcasts its load level — as well as the load level for all sector-carriers in its neighbor list — on the synchronous control channel. The server selection algorithm at the access terminal then uses not only FL channel quality and RL channel quality (DRCLock bit) but also the FL load level from the candidate serving sectors on each carrier. The server selection metric is modified to use the FL channel quality and the FL load level, and the constraint whereby the AT selects a serving sector from sectors with acceptable RL quality is maintained.

4 Single-Carrier Multilink

EV-DO ATs are multicarrier enabled, which means they can receive data on multiple links regardless of whether these links are from the same sectors on the same carrier. This capability can be harnessed with SCML to allow multicarrier-enabled ATs to have improved performance even in regions of the network with less than three carriers. Because SCML is beneficial only in handoff regions (typically characterized by lower SINR and less-than-ideal performance), it delivers gains where they are needed most. With SCML, the network can serve the AT using multiple servers on a

carrier. Each FL server creates a link between the AN and AT. SCML allows multiple links on a single carrier, and that is why it is called single-carrier multilink. An AT's active set are those sectors that control the power of the AT on the RL and can serve the AT on the FL. SCML enhances FL data rate when all sectors in the AT's active set are lightly loaded, and it balances the load when some chokepoint sectors are in the AT's active set. For an AT that can receive FL data from n links simultaneously, SCML allows the AN to assign additional links and enhance FL throughput when the number of carriers assigned to AT is $< n$ and the AT has multiple sectors in the active set. SCML leverages the advantages of EV-DO, and in the following, we explain some changes to existing EV-DO.

4.1 Reverse Link Feedback Multiplexing

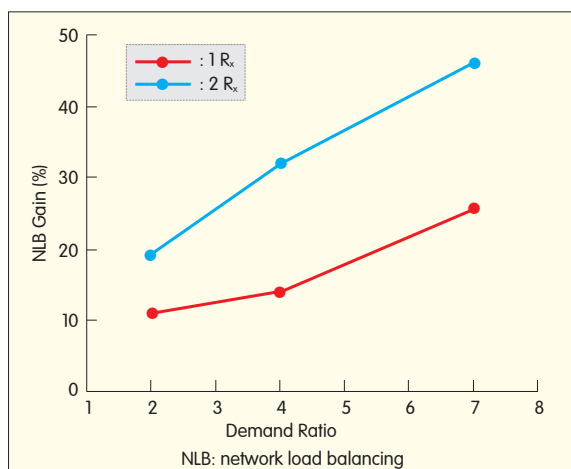
For each additional link assigned using SCML, an additional set of RL feedback channels is required. This is sent over a single RL carrier using reverse link feedback multiplexing. The multiplexing is supported by methods such as basic feedback multiplexing (BFM) and enhanced feedback multiplexing (EFM).

4.2 Distributed Network Scheduling

The network can more flexibly schedule FL data when an AT is served on multiple links. Distributed network scheduling (DNS) improves network efficiency by biasing FL data delivery towards a better link [4]. When FL slot use is 100%, DNS fairly schedules across all ATs regardless of the number of links assigned. When FL slot use is less than 100%, DNS allows SCML ATs to achieve some trunking gain by using free slots on each link, which results in a higher FL data rate for SCML ATs.

4.3 Receiving Diversity and Interference Nulling

An SCML AT may be simultaneously served from multiple links on same carrier, resulting in self interference. The AT is simultaneously served from two sectors that interfere with each other. Even if no other AT is present in the system, each link assigned to the



▲ Figure 3. NLB gain as a function of demand ratio.

SCML AT receives interference from another link(s). To achieve gains from multiple links, the AT must overcome the interference. Some EV-DO receiving diversity implementations can spatially null a strong interferer, and this is the key to SCML. The network should limit SCML assignment to receiving diversity ATs with spatial nulling capabilities. ATs with more Rx antennas are typically capable of superior spatial nulling of strong interferers, and therefore, SCML performance improves with an increase in number of AT Rx antennas.

4.4 Smart Carrier Management

The smart carrier management algorithm can be modified to take the SCML capability of a device into account. The network allocates and removes SCML based on signal conditions, and this ensures that additional links can provide reasonable throughput. Links across carriers are preferred because they are orthogonal and provide trunking (multiplexing) gain. If the AT can support more links than assigned carriers, AN uses SCML to assign additional links on a carrier according to available FL control resources and RL load on that carrier. The additional links provide trunking gain in the spatial dimension. Once the AT server selection algorithm has been assigned multiple links by the smart-carrier management algorithm, the AT server-selection algorithm chooses the best link(s) by using the FL

channel quality and FL load. This is similar to the NLB algorithm for new ATs. The AN has multiple paths that it can use to serve FL data, and DNS allows network throughput to be optimized.

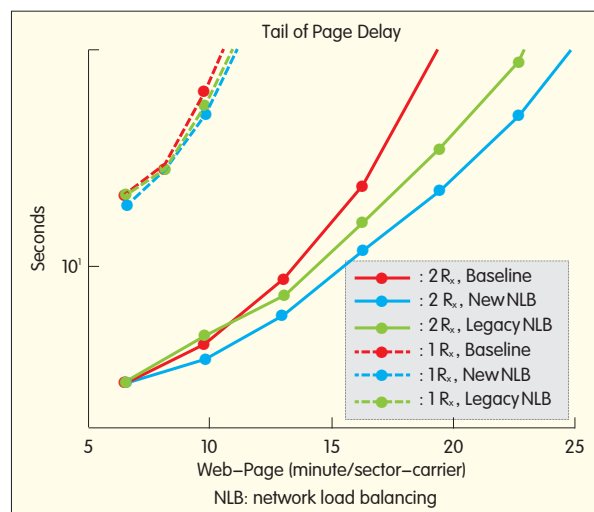
5 Performance

Simulations reveal the performance gained using NLB and SCML. The performance results are valid for a seven-cell layout with a center-cell demand model; that is, the center cell has multiple times the number of users of neighboring cells. The ratio of the number of users in the center cell to users in the neighboring cell is the demand ratio. Except for Fig. 3, which shows load-balancing gain as a function of demand ratio, all other figures are valid for a demand ratio of three. Users have an http traffic model; that is, they repeat downloading a sample http webpage according to a random arrival process with a fixed rate. To determine performance in a particular scenario, for example, dual-antenna or dual-carrier devices with load balancing enabled, simulations are performed for a range of download rates. Each simulation is then characterized in terms of download rate (the average number of webpages downloaded per minute per high-demand sector-carrier) and the tail of the page delay. The tail of the page delay is defined as follows: The delay for each downloaded http page is the time between when the first byte of the page is queued in the BSC to the time the last byte is downloaded by the user. Then, the page delay CDF (across all users and all webpages) is formed, and the ninety percentile delay is chosen as the tail page delay. The tail page delay

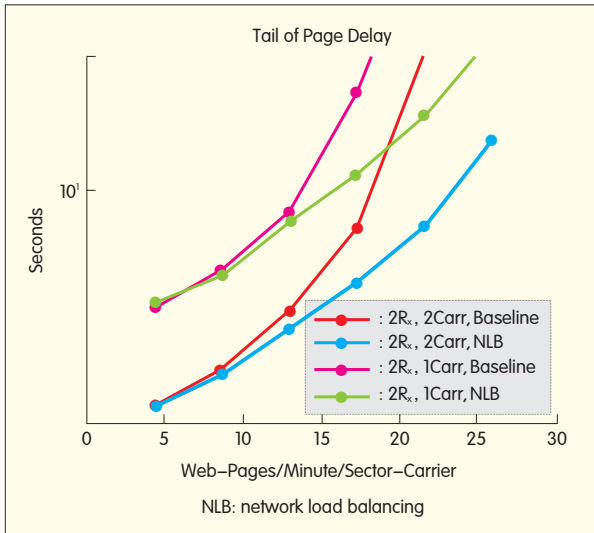
versus rate curve for the scenario is then formed from all such rate-delay pairs. Both single and dual-antenna devices are simulated. Single and multicarrier devices are also simulated.

5.1 Load-Balancing Gain for Single-Carrier Devices

Fig. 4 shows the tail page delay versus rate curves for single-carrier devices with one or two antennas. Load balancing provides significant gain only when the load level is sufficiently large, that is, when the solid red and blue curves (which represent the baseline and new NLB cases for two-antenna devices, respectively) fall on top of each other at low rates. Because of the low load differential at low load levels, no user is offloaded to another sector and there is no load balancing gain. Also in Fig. 4, the load-balancing gains for single-antenna devices (new or legacy) are not as large as those for dual-antenna devices. Once a user is offloaded from a heavily loaded sector to a lightly loaded one, the heavily loaded sector appears as a strong interferer. This occurs because the user receives a stronger signal from the heavily loaded sector than from the lightly loaded one. Dual-antenna devices can spatially null some of the interference. Single-antenna devices lack such capability and thus achieve lower load balancing gains. Multiple receiving antennas and special null of a



▲ Figure 4. NLB gain for single-carrier devices with one and two antennas (600 kB per web page).



▲ Figure 5. Load-balancing gain devices with two antennas (600 kB per web-page).

strong interferer becomes even more important for SCML because users usually suffer self-interference. Consequently, NLB and SCML are recommended only for dual-antenna devices.

Fig. 4 also shows that although the load-balancing gain for legacy devices is not as large as the gain for new devices, they are comparable. The gain is reduced because the BSC, which induces load balancing for legacy terminals, does not have accurate information about user SINR.

Fig. 3 shows that the load-balancing gain increases with the demand ratio, that is, the ratio of users in the center cell to users in the neighbor cell. This is a result of more users being offloaded from the heavily loaded center cell to the lightly loaded neighboring cells as the demand differential increases. Load balancing provides substantial gains over a wide range of demand ratios.

5.2 Load-Balancing Gain for Multicarrier Devices

Fig. 5 shows the tail page delay versus rate curves for single and multicarrier devices (the maximum number of assigned carriers is two). The single and multicarrier devices have two antennas. Load-balancing gain improves when a second carrier is added. As carriers are added, users experience trunking (multiplexing) gain.

The horizontal distance between the magenta and red curves in Fig. 5 represents the trunking gain of dual-antenna devices when a second carrier is added. Trunking gain is also a function of load level. As the load level increases, the trunking gain decreases. The magenta and red curves in Fig. 5 merge as rate is sufficiently increased. Both baseline and NLB cases achieve trunking gain when a second carrier is added; the trunking gain achieved in the latter case is more substantial

because some users hand off to lightly loaded neighbors.

In these cases, there is a dual benefit from NLB—spatial load-balancing combined with load-balancing in the frequency domain—and this magnifies the gains from spatial load balancing. NLB combined with multicarrier deployments increases network capacity when the network is loaded and also substantially improves UE. This means faster web-page downloads when the network is not as loaded.

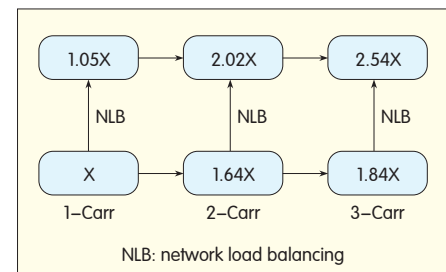
Fig. 6 and Fig. 7 show the relationship between load balancing and trunking gains for two-antenna devices at low (7 second tail page delay) and high (13 second tail page delay) load levels. Specifically, X in Fig. 6 denotes the network capacity for a single-carrier deployment with dual-antenna devices where the tail page delay does not exceed 7 seconds. The coefficients in Fig. 6 represent the per-carrier network capacity gain when load balancing is enabled or additional carriers are added. At low load levels, per-carrier trunking gain (63%) created by adding a second carrier is much larger than the gain from load balancing (5%). NLB provides significant gain when sectors are sufficiently loaded; trunking gain is greater when load level is smaller. In contrast, Fig. 7 shows that at high load

levels, load balancing provides the same gain (26%) as adding the second carrier. Thus, combining multicarrier deployments with per-carrier load balancing provides substantial gain over a wide range of load levels.

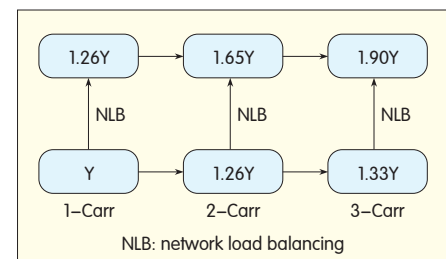
5.3 SCML Performance

Fig. 8 shows FL burst rate as a single-carrier user moves between two neighboring cells. With no SCML, a user's burst rate reduces as the AT moves away from the center of the cell and approaches the cell edge. The burst rate starts increasing again as the AT approaches the center of the neighboring cell. With SCML, a user's burst rate is significantly improved near the cell edge because the user is served by two sectors at the cell edge. Thus SCML can provide ATs with a more uniform UE as the user moves within the network.

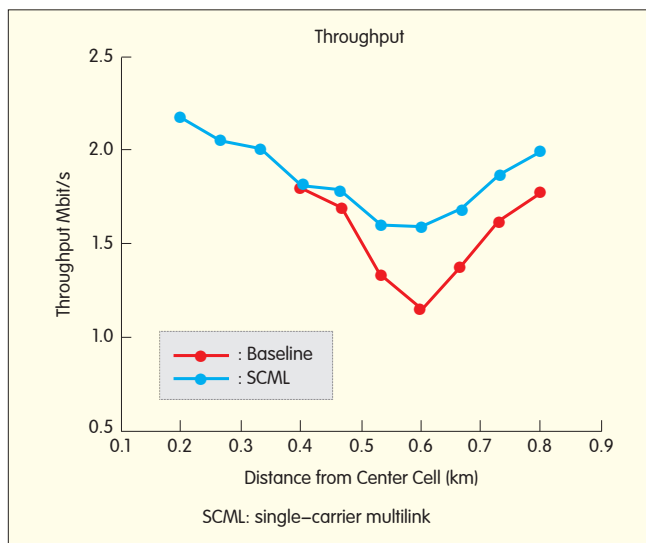
Fig. 9 shows the tail page delay versus rate curves for dual-antenna single-carrier devices. The cluster consists of seven sectors, and the center sector has three times the number of users of its neighboring sectors. Load balancing provides substantial gains only when load level is



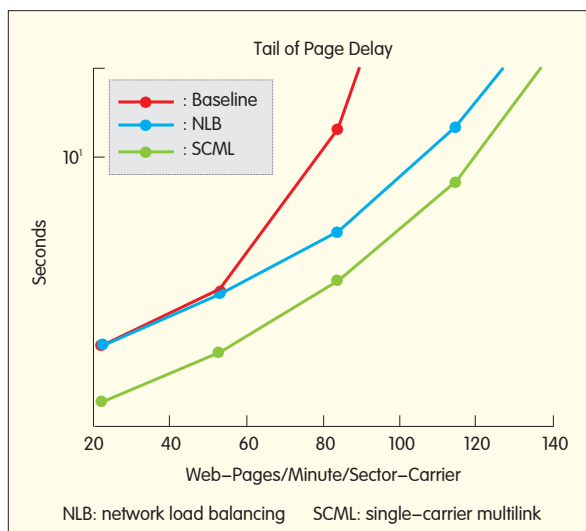
▲ Figure 6. NLB gains for dual-antenna multicarrier devices at a low load level (7 second tail page delay).



▲ Figure 7. NLB gains for dual-antenna multicarrier devices at a high load-level (13 seconds tail page delay).



◀ Figure 8. Burst rate for a single-carrier user moving between two neighboring cells.



▲ Figure 9. SCML gain for dual-antenna single-carrier devices (300 kB per webpage).

high, whereas SCML provides substantial gains at all load levels. At low load levels, SCML exploits spatial trunking across sectors, whereas at high load levels, SCML asymptotes to NLB where the AT is effectively served by one sector only. Single-carrier multilink is therefore a form of soft-network load balancing.

6 Conclusions

This paper gives an overview of load balancing in the spatial dimension. NLB and SCML are introduced, and related algorithms, implementation, and performance are presented. We also

show that load balancing in the spatial dimension and frequency dimension can be combined to amplify gains in networks where capacity is constrained. The proposed methods are fully backward compatible and leverage the advantages of EV-DO networks thus increasing the return on investment for these networks. NLB, in particular, is applicable to legacy devices. These techniques improve user experience when the sector is not operating at load.

Further improvements to NLB and SCML can be

made with higher-order receiving diversity at the device. This enables further improvements in spatial nulling, which allows the device to be simultaneously served by even more sectors on the same carrier.

Similar techniques, such as single-frequency dual cell (SFDC), are being developed for UMTS networks and are applicable to LTE networks as well. NLB and SCML are both applicable to local-area wireless networks.

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AD Index

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Uplink Power Control for MIMO-OFDMA Cellular Systems

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Abstract: In this paper, we propose a novel uplink power control algorithm, SMST, for multiple-input multiple-output orthogonal frequency-division multiple access (MIMO-OFDMA). We perform an extensive system-level simulation to compare different uplink power control algorithms, including the FPC adopted in 3GPP LTE and LTE-Advanced. Simulations show that SMST adopted in IEEE 802.16m outperforms other algorithms in terms of spectral efficiency, cell-edge performance, interference control, and trade-off control between sector-accumulated throughput and cell-edge user throughput. The SMST performance gain over FPC can be more than 40%.

Keywords: uplink power control; inter-cell interference; OFDMA; MIMO

1 Introduction

Uplink power control is a critical feature of CDMA cellular systems. It is used to alleviate the near-far problem caused by intracell interference. The new generation of broadband wireless technologies, including WiMAX and LTE, are designed to provide higher bandwidth, higher peak throughput, and higher spectral efficiency [1],[2]. These wireless technologies are based on orthogonal frequency-division multiple access (OFDMA), in which all the uplink transmissions are orthogonal within one cell [3]. Therefore, intracell interference is minimal compared with technologies based on 3G CDMA.

Fourth-generation WiMAX and LTE wireless standards are designed to support up to 20 MHz channel bandwidth, high-order 4×2 and 4×4 multiple-input multiple-output (MIMO), and aggressive frequency reuse (reuse 1) to improve spectral efficiency and user throughput. Especially for cell-edge users, intercell interference is a significant problem caused by aggressive frequency reuse. Uplink power control is an important

mechanism for controlling intercell interference and improving cell-edge user experience (UE), even in broadband wireless systems based on OFDMA[4]–[7]. As opposed to 3G, where closed-loop power control is typically used to control both intracell and intercell interference, the main objective of uplink power control in OFDMA-based systems is to control intercell interference [8],[9].

In this paper, we investigate control of uplink transmit power in order to maximize sector and cell-edge spectral efficiency. These are essential parameters for next-generation broadband wireless systems [10]–[13]. A simplified maximum-sector throughput (SMST) algorithm is proposed that maximizes sector throughput by adjusting uplink transmit power.

2 Uplink Power Control Mechanisms

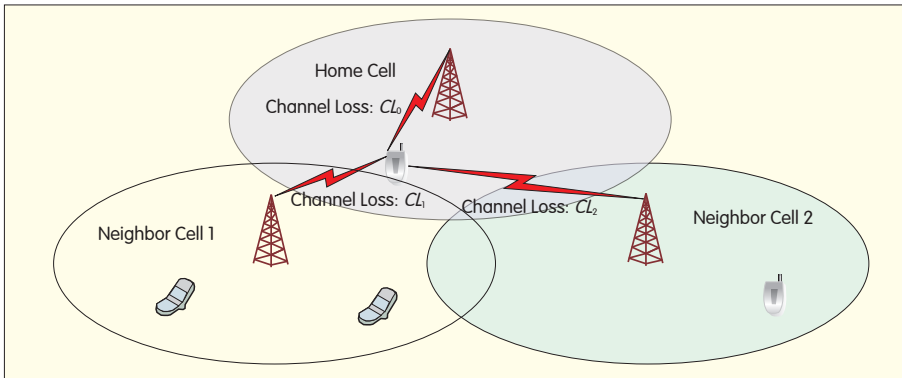
2.1 Background

Power control has been studied extensively since the introduction of cellular systems. A power-control

mechanism can be closed-loop power control (CLPC), open-loop power control (OLPC), or CLPC-OLPC combined power control. In CLPC, power control is centralized at the base station (BS). The mobile station (MS) provides feedback on link quality, and the BS calculates the uplink transmit power level for the MS and instructs the MS to transmit at that level. In OLPC, the MS measures link quality and calculates the uplink transmit power level (based on predetermined equations) in a distributed manner. The BS may influence the MS by adjusting certain parameters in the equation, but the BS does not directly control the MS transmit power.

2.1.1 CLPC

In a CDMA system, CLPC allows commands to be sent from the BS so that power can be quickly adjusted. In an OFDMA system, intracell interference is not significant, so adaptive modulation and coding (AMC) and hybrid automatic repeat request (HARQ) are used to provide fast link adaptation for the data channel. CLPC is mainly used for fixed-rate control channel when channel fading exceeds



▲ Figure 1. Uplink interference for one MS in a typical MIMO-OFDMA cellular system.

the power margin. In CLPC in the BS, the received signal quality is monitored and power-adjustment commands are sent.

2.1.2 OLPC

OLPC is mainly implemented in the MS. The MS measures downlink signal status, compensates the uplink path loss, and controls interference to neighboring BSs. With OLPC, the MS needs some static/semi-static configuration parameters to be signaled by the BS and does not require short-term inputs. This saves overall signaling overhead.

2.1.3 CLPC-OLPC Combined Power Control

In current 4G wireless standards, both CLPC and OLPC are combined to balance flexibility with signaling overhead. OLPC is mostly used to save signaling overhead.

2.2 Uplink Power Control Algorithms

Depending on the goal of the power control mechanism, the uplink power-control algorithm can be based on signal-to-noise ratio (SNR), signal-to-interference plus noise ratio (SINR), or Internet of things (IoT).

2.2.1 SNR-Based Algorithm

The goal of an SNR-based algorithm is to maintain the desired received signal strength in the BS. An SNR-based algorithm does not take into consideration the uplink-received interference power level. This type of algorithm is simple to implement and always convergent. Fractional power

control (FPC) in LTE is an SNR-based algorithm.

2.2.2 SINR-Based Algorithm

The goal of an SINR-based algorithm is to maintain the desired received SINR level in the BS while taking into account the uplink interference power level. SMST used in IEEE 802.16m is an SINR-based algorithm that defines the desired received SINR goal for each MS and takes into account the measured downlink signal-to-interference ratio (SIR), uplink MIMO mode, and BS antenna configuration.

2.2.3 IoT-Based algorithm

The goal of an IoT-based algorithm is to maintain the desired uplink interference level in the BS. In general, an IoT-based algorithm can stabilize the interference level in the uplink to help control interference and modulation-coding-scheme (MCS) level estimation.

3 Maximizing Throughput with Power Control

3.1 System Modeling

Fig. 1 shows an uplink interference model for one MS in a typical MIMO-OFDMA cellular system.

At any time, the MS uses the uplink to transmit to its home BS and causes interference to neighboring BSs. To simplify the analysis, simple input simple output (SISO) is assumed, and the parameters for the model are

- P_s : The MS uplink transmission

power (linear) of one data subcarrier at a given time;

- i : cell index. $i = 0$ is the home BS, and $i = 1-N$ is the neighboring BSs;
- CL_i : The instantaneous channel loss (linear) from MS transmitter to one receiving antenna of a BS;
- N/I : The noise-plus-interference level (linear) per subcarrier at a BS receiving antenna.

3.2 Maximum Throughput Criteria

The aggregated cell throughput is

$$R_{\text{Aggregated}} = \sum_i R_i \quad (1)$$

If we assume that all BSs occupy the same bandwidth, (1) can be modified:

$$\begin{aligned} R_{\text{Aggregated}} &= \sum_i BW \times SE_i = BW \times \sum_i SE_i \\ \overrightarrow{SE}_{\text{Aggregated}} &= \sum_i SE_i \end{aligned} \quad (2)$$

For uplink power control of each MS, aggregated spectrum efficiency SE is prioritized as the target of the algorithm, which can be expressed as

$$P_{tx} = \arg\max_{P_{tx}} \sum_i SE_i \quad (3)$$

To solve (3) for each MS, the following process is used:

- 1) P_s is the transmission power of one subcarrier that is initialized to 0
- 2) A power increase, ΔP_s , is assumed in order to calculate

i) SE_{gain} : as the power increases, this is the spectrum efficiency gain that the MS can achieve in the home BS on the subcarrier.

ii) SE_{loss} : as the power increases, this is the spectrum efficiency loss the MS inflicts on the neighboring BSs on the subcarrier.

3) SE_{gain} and SE_{loss} are compared

i) If $SE_{\text{gain}} > SE_{\text{loss}}$, $P_s = P_s + \Delta P_s$, go back to 2

ii) If $SE_{\text{gain}} \leq SE_{\text{loss}}$, then the PS is optimum on the subcarrier for the MS.

This process is used to evaluate the SE_{gain} and SE_{loss} for each power increase of ΔP_s .

At any time, when a power increase of ΔP_s is assumed, the SE_{gain} of the MS on the subcarrier can be obtained by

$$SE_{\text{gain}} = \log(1 + \text{SINR}(\text{Home})_{\text{New}}) - \log(1 + \text{SINR}(\text{Home})_{\text{Original}}) \quad (4)$$

where

$$SINR(Home)_{Original} = \frac{\frac{P_s}{CL_0}}{NI_0} \quad (5)$$

$$SINR(Home)_{New} = \frac{\frac{(P_s + \Delta P_s)}{CL_0}}{NI_0} \quad (6)$$

Combining (4), (5), and (6), SE_{gain} can be expressed as

$$SE_{gain} = \log \left(1 + \frac{\frac{\Delta P_s}{CL_0}}{NI_0 + \frac{P_s}{CL_0}} \right). \quad (7)$$

The SE_{loss} on the subcarrier in one neighbor BS, ($i = 1-N$) can be expressed as

$$SE_{loss}(i) = \log(1 + SINR(i)_{Original}) - \log(1 + SINR(i)_{New}). \quad (8)$$

where $SINR(i)_{Original} = \frac{S_i}{NI_i}$,

$$SINR(i)_{New} = \frac{S_i}{NI_i + \Delta I_i},$$

S_i is the received signal power on the subcarrier of BS_i , and $\Delta I_i = \frac{\Delta P_s}{CL_i}$ is the increased inference power caused by ΔP_s .

From (8), the total SE_{loss} on the subcarrier in all neighbor BSs can be expressed as

$$SE_{loss} = \sum_{i=1}^N SE_{loss}(i). \quad (9)$$

Therefore, the optimum power on the subcarrier can be calculated by increasing P_s of the subcarrier by ΔP_s steps from 0 until the SE_{gain} and SE_{loss} on this subcarrier no longer satisfies

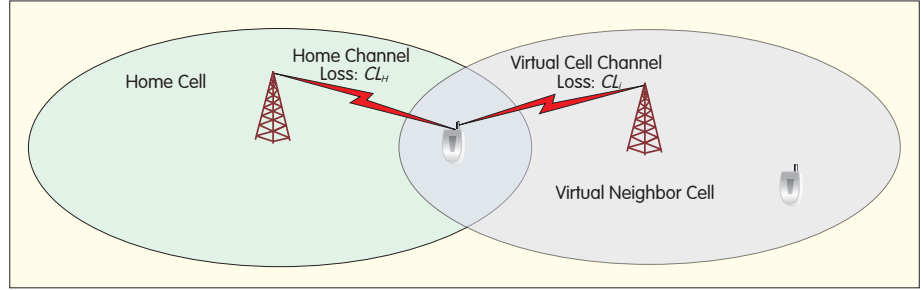
$$SE_{gain} \geq SE_{loss}. \quad (10)$$

If the MS is assigned resources for uplink transmission by the BS, optimal transmission power for all assigned uplink subcarriers can be calculated in order to achieve the overall optimum cell throughput. This algorithm is called the maximum sector throughput (MST) algorithm.

4 Simplified Maximum Sector Throughput Algorithm

4.1 MST Algorithm Simplified Form

The MST algorithm is only useful in



▲ Figure 2. Uplink interference from one MS.

theory and is impossible to be implemented in practice. The algorithm requires the home BS or MS to accurately know the received signal power and interference power on all neighbor BSs on each subcarrier at the time of uplink transmission. Making some simple assumptions, we developed a practical SMST algorithm. First, we modeled one virtual neighbor BS (or sector) that accounts for all interference impact on SE_{loss} (Fig. 2).

We assume that all BSs have the same downlink transmission power level. The total downlink reference interference power from the virtual BS to the MS is

$$P_{DL,I} = \frac{P_{DL,Preamble}}{CL_I} = \sum_{i=1}^N \frac{P_{DL,Preamble}}{CL_i} \quad (11)$$

where $P_{DL,Preamble}$ is the downlink preamble power used as the reference signal to measure downlink path loss, and CL_I is the virtual downlink path loss. The downlink reference signal power of the MS is

$$P_{DL,S} = \frac{P_{DL,Preamble}}{CL_H}. \quad (12)$$

Downlink SIR can be measured as

$$SIR_{DL} = \frac{P_{DL,S}}{P_{DL,I}}, \text{ so that } SIR_{DL} = \frac{CL_I}{CL_H}. \quad (13)$$

The SE_{gain} can be expressed as

$$SE_{gain} = \log \left(\frac{1 + SINR_{New,MRC}}{1 + SINR_{Original,MRC}} \right). \quad (14)$$

One virtual neighbor model is used, and one MS keeps the same transmission power spectral density (PSD) for all data tones (PSD_{Data}). Only one transmission stream is used, and there are N_r receiving antennas at the

BS (an MRC receiver is assumed).

It is further assumed that each receiving antenna on the BS suffers similar noise and interference level $NI_{H,Ant}$, and the path loss from transmission antenna to each receiving antenna is similar to CL_H , then (14) can be re-written as

$$SE_{gain} = \log \left[\frac{1 + \frac{N_r \times (PSD_{Data} + \Delta PSD_{Data})}{CL_H \times NI_{H,Ant}}}{1 + \frac{N_r \times PSD_{Data}}{CL_H \times NI_{H,Ant}}} \right] = \log \left[1 + \frac{\frac{\Delta PSD_{Data}}{CL_H}}{NI_{H,Ant} + \frac{N_r \times PSD_{Data}}{CL_H}} \right]. \quad (15)$$

Similarly, the new SE_{loss} on the virtual neighbor BS can be expressed as

$$SE_{loss} = \log \left(\frac{1 + SINR'_{Original,MRC}}{1 + SINR'_{New,MRC}} \right) = \log \left[\frac{1 + \frac{N_r \times SNR_{I,Ant} \times P_{Noise,Ant}}{NI_{I,Ant}}}{1 + \frac{N_r \times SNR_{I,Ant} \times P_{Noise,Ant}}{NI_{I,Ant} + \frac{\Delta PSD_{Data}}{CL_I}}} \right] \quad (16)$$

where $NI_{I,Ant}$ is the noise plus interference for each antenna on the virtual BS, $P_{Noise,Ant}$ is the white noise for each antenna on the virtual BS, $SNR_{I,Ant}$ is the average SNR level for each antenna on the virtual BS, and $SNR_{I,Ant} \times P_{Noise,Ant}$ is used to estimate received signal PSD for each antenna on the virtual BS.

The optimum overall SE can be obtained when the following condition is met:

$$\max_{\Delta PSD_{Data} \rightarrow 0} (SE_H + SE_I) \Rightarrow \Delta SE = SE_{gain} - SE_{loss} = 0 \quad (\Delta PSD_{Data} \rightarrow 0). \quad (17)$$

From (13), (15), (16) and (17), we can

derive

$$SINR_{H,Ant} = \frac{NI_{I,Ant}}{NI_{H,Ant}} \times \left(1 + \frac{1}{N_r \times SINR_{I,Ant}}\right) \times \left(SIR_{DL} - \frac{1}{N_r}\right) \quad (18)$$

where, $SINR_{H,Ant}$ is the received average SINR for each antenna on the home BS, and

$$SINR_{I,Ant} = \frac{SIN_{I,Ant} \times P_{Noise,Ant}}{NI_{I,Ant}}.$$

Equation (18) can be further simplified:

$$SINR_{H,Ant} = \gamma \times SIR_{DL} - \frac{1}{N_r} \quad (19)$$

where γ is a derived parameter to control the interference to other cells:

$$\gamma = \frac{NI_{I,Ant}}{NI_{H,Ant}} \times \left(1 + \frac{1}{N_r \times SINR_{I,Ant}}\right). \quad (20)$$

The parameter, γ , is linearly related to the ratio of virtual-cell average NI level to home-cell average NI level. High γ results in high interference over thermal (IoT), and low γ results in low IoT.

4.2 Limitation of Minimum Transmission Rate

Equation (19) provides the optimal solution for the SMST algorithm. The resulting target SINR on each antenna is expressed as a linear value. From (19), some MSs could have negative target SINR because of the very low measured downlink SIR. For these MSs, the results of (19) indicate that any power assigned to these MSs reduces overall throughput. Because all active MSs must support a minimum transmission rate to keep them online, the minimum target SINR (to support the minimum transmission rate) should be set as the threshold. Then, (19) is modified as follows:

$$SINR_{Target} = 10 \log_{10} \left(\max \left(10^{\frac{SINR_{MIN}}{10}}, \gamma \times SIR_{DL} - \frac{1}{N_r} \right) \right). \quad (21)$$

In (21), the resulting target SINR is converted to decibels so that the transmission power can be conveniently calculated. The minimum SINR threshold is expressed in decibels

and is converted into a linear value to align with the linear result of (19). Equation (21) is a core part of the IEEE 802.16m [3] uplink power-control algorithm.

Equation (21) is the SMST algorithm combined with minimum target SINR threshold. It expresses the suitable uplink target SINR in each receiving antenna on a home BS. If OLPC is applied, the PSD of each data subcarrier used by the MS is

$$PSD_{Tx} = L + SINR_{Target}(\text{dB}) + NL + Offset \quad (22)$$

where L is the average downlink path loss measured by MS base on BS transmission power level and received signal power level, NI is the average noise and interference level for each subcarrier at the BS antenna, the information is broadcasted from BS to MS, and $Offset$ is the MS-specific power offset decided by the BS.

If (21) is used for conventional CLPC design, MS needs to report the measured downlink SIR value SIR_{DL} to BS periodically, and BS then uses (21) to calculate the target SINR. Compared with the measured SINR, the difference is compensated by CLPC commands.

Equation (21) is the solution for uplink single stream. In IEEE 802.16m [11], two options for uplink multistream power control were discussed. The power level of each stream in uplink multistreams can be kept the same as the single stream or the power level of each stream in uplink multistreams can be reduced to keep the sum of power/interference similar to the single stream. Both options improve performance in different cell sizes and in different scenarios, so there is one additional control parameter added into (18) to support both options:

$$SINR_{Target} = 10 \log_{10} \left(\max \left(10^{\frac{SINR_{MIN}}{10}}, \gamma \times SIR_{DL} - \frac{1}{N_r} \right) \right) - \beta \times 10 \log_{10}(TNS) \quad (23)$$

where β is the newly added parameter and can be set by the BS as 0 (disabled) or 1 (enabled) for environment performance tuning. TNS is the total number of uplink multistreams.

Equation (23) is the final derivation of SMST adopted into IEEE 802.16m [3] for data-channel power control. 16 m control-channel power-control design was discussed in [14].

5 Algorithm Evaluation and Comparison

5.1 Evaluation Considerations

Before evaluating uplink power control algorithms, the following general points for system-level simulation need to be considered:

- sector-cumulated throughput and cell-edge throughput. These are the metrics of overall performance determined by uplink power-control algorithms.

- fairness control curve. In general, the uplink power control algorithm provides a trade-off between sector-cumulated throughput and cell-edge throughput. One new-form curve is used to show the sector SE and cell-edge SE (Figs. 3, 4, 8 and 9).

- IoT control. IoT is the key metric of uplink interference in a system evaluation. Effective IoT control needs to be proven for an uplink power control algorithm.

As (22) and (23) show, there are some key parameters that need to be evaluated and discussed for real implementation:

- γ plays a key role in IoT and fairness. In the evaluation, the results of different γ values are discussed

- $SINR_{MIN}$ (dB) is the minimum threshold for cell-edge user SINR.

- L is the average downlink path-loss measured by the MS. This is key to deciding the transmission power level. For different product implementations, the long-term average or short-term average have cause different effects.

- The open-loop power adjustment is decided by the MS. The rate of power control may be used in product implementation. Fast (per-frame) or slow (per 50 frames) control rates are evaluated.

5.2 Results and Discussion

The evaluation scenario in [15]

▼ Table 1. Key parameters for IEEE 802.16 m ULPC evaluation scenario

Parameter	Value
Site Layout	Hexagonal Grid, 19 3-Sector Sites, Wrap-Around
Carrier Frequency(GHz)	2.5
System Bandwidth(MHz)	10
Reuse Factor	1
Frame Duration (Preamble+DL+UL)(ms)	5
Number of OFDM Symbols in UL Frame	18
FFT Size(tones)	1024
Useful Tone	864
Number of LRU	48
LRU Type	DRU
Number of Users per Sector	10
CMIMO Support	No
User Location	Uniform Distribution
Site to Site Distance(m)	500
Channel	eITU-Ped B, 3 km/h
Max Power in MS(dBm)	23
Antenna Configuration	1 × 2 SIMO
HARQ	On (Max Retrans: 4/Sync)
Target PER	0.2
Link to System Mapping	RBIR
Schedule Type	PF
Resource Assignment Block	8 LRU
Penetration Loss(dB)	20
Control Overhead	0 for SE Calculation (not Defined yet)

CMIMO: Collaborative MIMO
 DRU: Distributed Resource Unit
 HARQ: hybrid automatic repeat request
 LRU: least recently used
 RBIR: Resource Block Information Rate
 SIMO: Single-Input-Multi-Output

follows the IEEE 802.16m Evaluation Methodology Document [16], but some simplifications are made for uplink power control. The key parameters of the evaluation scenario are listed in Table 1.

In the OLPC algorithm, path loss and power control rate are related to implementation. The path loss L is applied to (22) to calculate the transmission power for each subcarrier. L is estimated by the MS through downlink signaling measurement. For the extreme evaluation setting, the path loss L is assumed with two conditions:

- instantaneous path loss. This is the ideal accurate instantaneous (current

▼ Table 2. Evaluation results of different gamma values

Gamma	$SINR_{MIN}$ (dB)	Sector Throughput(Mbit/s)	Cell-Edge Throughput(kbit/s)	Sector SE	Cell-Edge SE
0	0	2.7083	256.5689	0.7222	0.0684
0.2	0	3.2387	262.6901	0.8636	0.0701
0.4	0	3.7738	252.3136	1.0064	0.0673
0.6	0	4.1149	222.1170	1.0973	0.0592
0.8	0	4.5482	180.5995	1.2129	0.0482
1.0	0	4.7901	150.1525	1.2773	0.0400
1.2	0	4.9155	102.1269	1.3108	0.0272
Full Power(No PC)	N/A	3.3585	32.5632	0.8956	0.0087

frame) downlink value used in the simulation

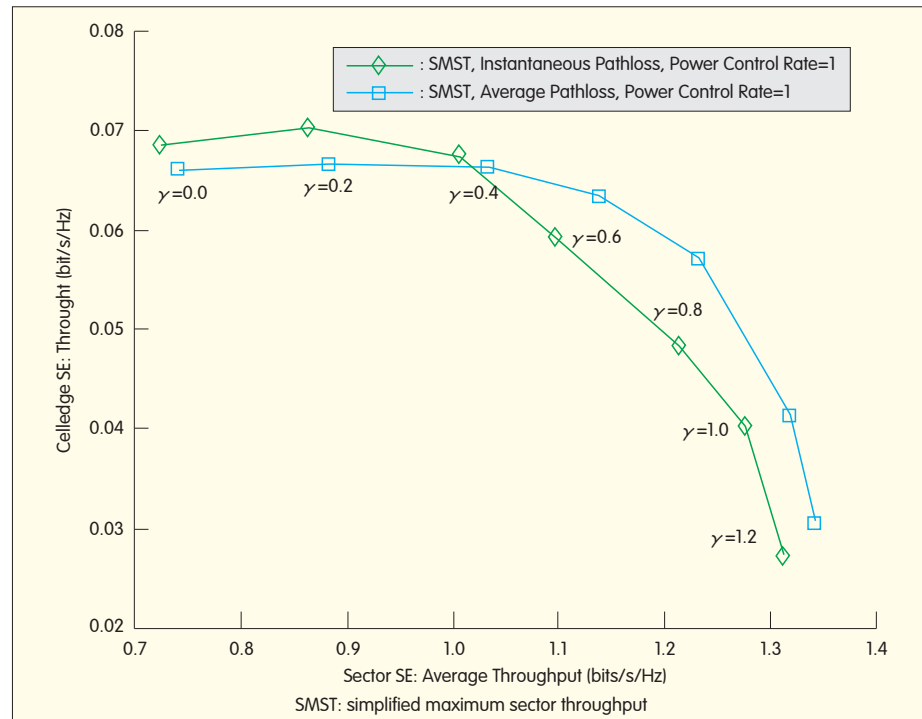
- average path loss. This is the estimated path loss is the very long-term (~50 frames, smoothing factor = 0.02) average downlink path loss. Ideally, short-term fast fading is smoothed.

In product implementation, the path loss for a specific product should be somewhere between the two extremes, depending on the averaging factor. The $SINR_{MIN}$ (dB) is set as 0 dB, and the results are shown in Table 2.

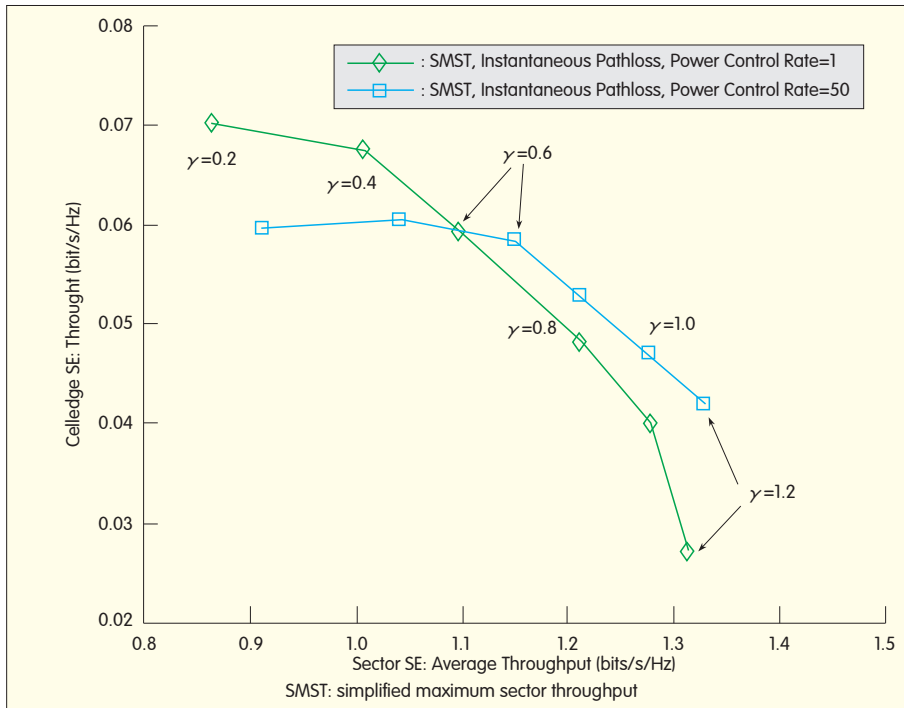
With different γ values, the performance trade-off between sector SE and cell-edge SE is shown in Fig. 3

based on the results of Table 2.

For OLPC, the power adjustment rate based on (22) can be per frame (rate = 1) or infrequent (rate > 1). In general, the power control rate is assumed to be 1; that is, in each frame, OLPC is applied for uplink transmission. However, there are some parameters related to product implementation, such as path loss, L , and downlink signal versus interference SIR_{DL} measurement and estimation. N /updating, broadcast by the base station, is not performed per frame. The change of power dictated by OLPC may be longer than one frame. Therefore, in one extreme case, a control rate of 50 frames is also



▲ Figure 3. Performance tradeoff curves: instantaneous path loss vs. averaged path loss. The calculation of sector spectrum efficiency (SE) and cell-edge SE is defined in [16].



▲ Figure 4. Performance tradeoff curves: control rate of 1 vs. control rate of 50.

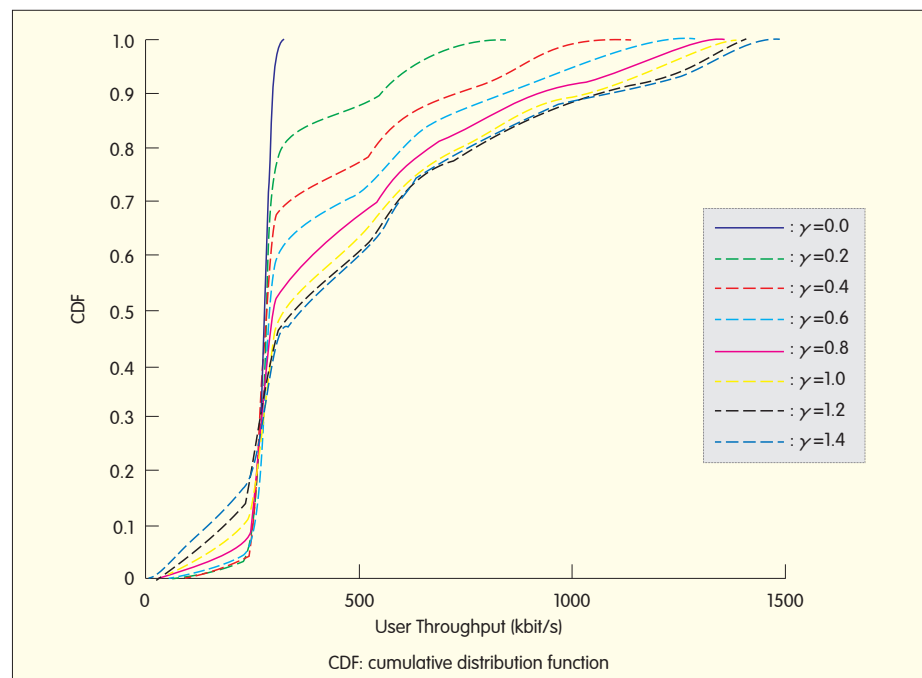
simulated to verify the robustness of the SMST algorithm.

In Fig. 3 and Fig. 4, the robustness of SMST compared with path-loss estimation and power updating rate is very clear. The average path loss shows minor gain in sector average throughput but minor loss in cell-edge SE. The reason is that the estimated average path loss can help the MS maintain stable transmission power that is determined by OLPC. Then, the signal/interference estimation on the BS is more accurate, and this is very important for the adaptive and modulation coding (AMC) process to assign the desired MCS level to the MS. The average path loss shows minor loss in a cell-edge SE because instantaneous path-loss estimation allows the MS to perform fast-link adaption by OLPC power change. Similarly, Fig. 4 shows that a slow power-updating rate of 50 has some gain in maximum sector SE and some loss in cell-edge SE.

Other aspects of uplink power control, such as user throughput distribution, IoT control, and power distribution, are shown in one of the following four cases, because it is

closely related to real product implementation. The evaluation results are presented as an empirical cumulative distribution function (CDF).

Fig. 5 shows one example of how the control factor, γ , controls the trade-off



▲ Figure 5. User throughput CDF by control factor γ .

between sectors to accumulate throughput and fairness in cell-edge performance.

The IoT distribution shows the effectiveness of interference management.

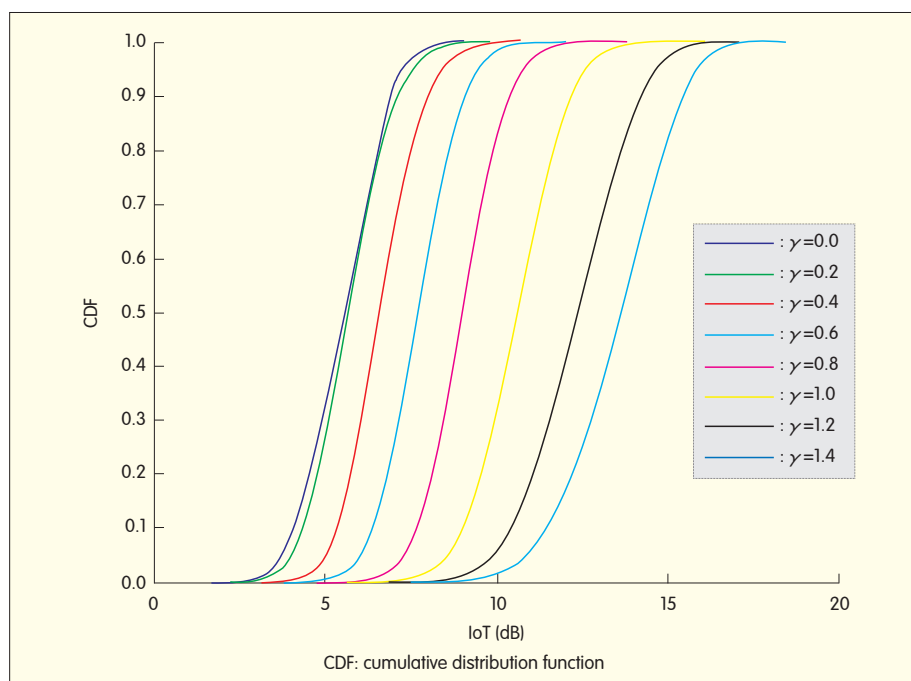
Fig. 6 shows the relationship between IoT distribution and control factor γ . When $\gamma = 0$, the SMST algorithm degenerates to a fixed SINR target method:

$$SINR_{\text{Target}} = SINR_{\text{MIN}} \text{ (dB)}. \quad (24)$$

The IoT distribution of $\gamma = 0$ is the minimum IoT value in the case where all MSs try to maintain the minimum transmission rate expected by the BS. The IoT value, an important measurement for intercell interference control, is jointly decided by $SINR_{\text{MIN}}$ (dB) and γ . The $SINR$ (dB) determines the base value of IoT distribution, and γ determines the IoT differential based on the base value. Fig. 7 shows IoT distribution for different $SINR_{\text{MIN}}$ values for $\gamma = 0.2$.

5.3. Comparison of Different Uplink Power Control Algorithms

In this section, we compare the performance of SMST with fractional power control (FPC) that was



▲ Figure 6. IoT CDF by control factor γ .

incorporated into 3GPP E-UTRA after Release8.

During the development of 3GPP LTE specifications, FPC was proposed [18]–[20] and used [17] as an OLPC method for uplink data channel physical uplink shared channel (PUSCH).

The key to FPC is to compensate the fraction of the path loss by control factor α , which can be expressed as PSD of each subcarrier, the same as in (22):

$$PSD_{Tx} = P_0 + \alpha \times PL. \quad (25)$$

When $\alpha = 0$, the FPC algorithm degenerates to a fixed transmission PSD algorithm without affecting path loss. When $\alpha = 1$, the FPC algorithm provides full path loss compensation and degenerates to the fixed target received signal strength (RSS) algorithm. The 3GPP specification [19] defines α from 0 to 1 as $\alpha \in \{0, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1\}$. The parameter, P_0 , is also important in FPC algorithm. The P_0 is mainly defined in two ways. In the first method of P_0 selection, α is fixed as one selected optimum value, such as 0.8, in most published results, and P_0 is searched for the optimum value in each simulation scenario. P_0 is explicitly signaled by eNodeB [21], [22] with a

large range.

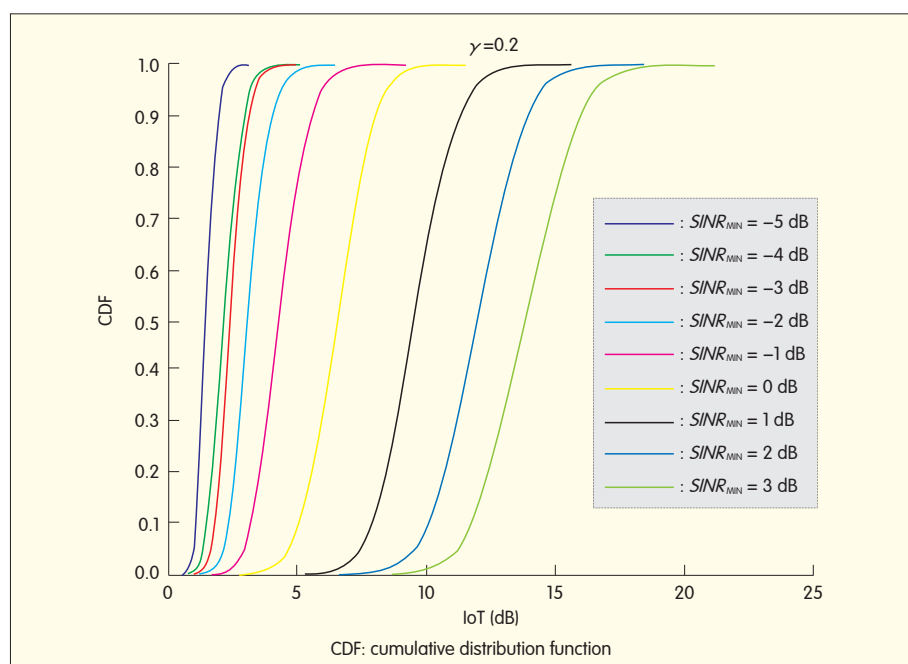
For the scenario defined in Table 1, the results of SMST and FPC are shown on Fig. 8.

The performance trade-off of FPC is located in the range of P_0 larger than -79 dBm. If the P_0 is not well selected, for example, when $P_0 < -79$

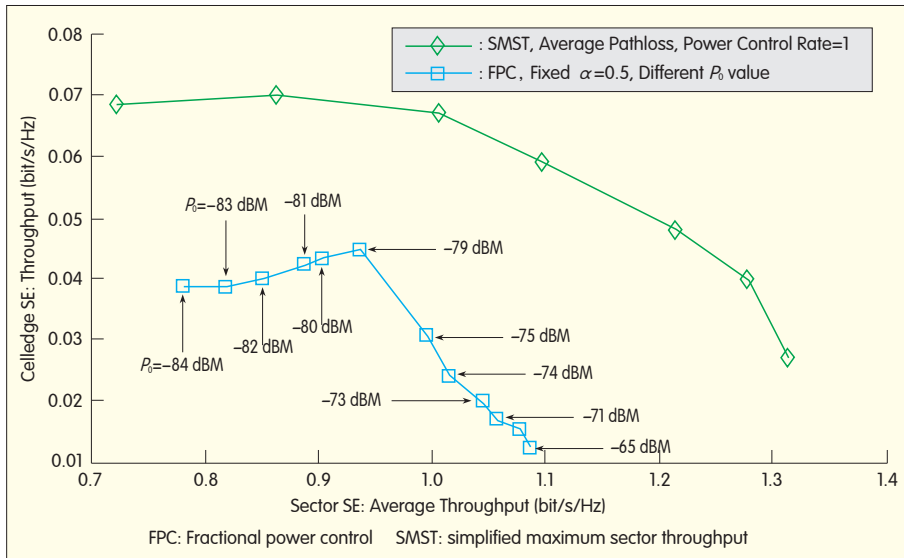
dBm, the sector SE and cell-edge SE degrades at the same time. Similar evaluation results can be found in [23] and [24], where the performance of sector throughput and cell-edge throughput are shown separately by IoT level. Here, the IoT level is directly controlled by P_0 .

When the selected optimum performance point of FPC is $P_0 = 79$ dBm with fixed $\alpha = 0.8$, the sector SE is 0.9375, and cell edge SE is 0.0447. Compared with the SMST algorithm results without optimum searching for $SINR_{MIN}$ (the value is just set as 0 dB), there is still big performance gap. If SMST maintains the same sector SE as FPC optimum point of 0.9375, the SMST can provide cell-edge SE of 0.0687, which is a 53.69% gain over 0.0447 of FPC optimum cell-edge SE. If SMST maintains the same cell-edge SE as FPC optimum point of 0.0447, the SMST can provide sector SE of 1.2404, which is a 32.31% gain over the 0.9375 of FPC optimum-sector SE. The average performance gap between SMST and FPC is 43%. In the second method of P_0 selection, P_0 is transformed from α value and cell-edge target SNR, as suggested in [23] and given by

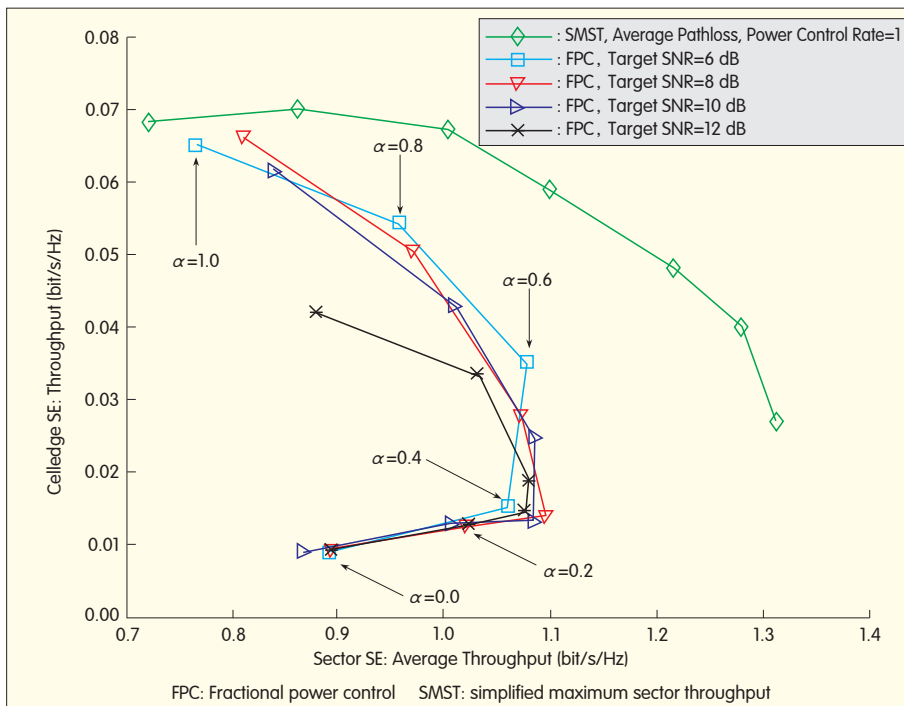
$$P_0 = \alpha \times (SNR_{Target} + PSD_n) + (1 - \alpha) \times PSD_{Max} \quad (26)$$



▲ Figure 7. IoT CDF by control factor $SINR_{MIN}$.



▲ Figure 8. Comparison of SMST and FPC performance curves (with fixed $\alpha = 0.8$).



▲ Figure 9. Comparison of SMST and FPC performance (with fixed-target SNR).

where SNR_{Target} is the cell edge target SNR, PSD_n is the thermal noise PSD, and PSD_{Max} is the maximum transmission power PSD for assigned resource size.

Equation (26) provides the connection between α and P_0 . As a result, if $\alpha = 0$, then (25) becomes

$$PSD_{Tx} = PSD_{Max} \quad (27)$$

FPC degenerates to a maximum transmission power scheme. If $\alpha = 1$, then (25) becomes

$$PSD_{Tx} = SNR_{Target} \quad (28)$$

FPC degenerates to a fixed receiving-target SNR method. A comparison of the performances of fixed-target SNR is shown in Fig. 9. In Fig. 9, the optimal performance

point of FPC algorithm is difficult to identify. One selected performance point for FPC ($SNR_{Target} = 6$ dB, $\alpha = 0.6$) is used for performance comparison, its sector SE is 1.0799, and its cell-edge SE is 0.0350. If SMST maintains the same sector SE as FPC selected point of 1.0799, the SMST can provide cell-edge SE of 0.0607, which is a 73.43% gain over 0.0350 of FPC selected cell-edge SE. If SMST maintains the same cell-edge SE as FPC optimum point of 0.0350, the SMST can provide sector SE of 1.2904, which is 19.49% gain over 1.0799 of FPC selected sector SE. Also, the average gain of SMST compared with FPC can be as much as 46.46%. From Fig. 8 and Fig. 9, SMST performs 40% better than FPC.

6 Conclusion and Discussion

In this paper, we have proposed a novel uplink power control algorithm, SMST, for MIMO-OFDMA systems. We also performed extensive system-level simulations to compare different uplink power control algorithms, including the FPC adopted in 3GPP LTE and LTE-Advanced. Our results show that SMST adopted in IEEE 802.16m outperforms other algorithms in terms of spectral efficiency, cell-edge performance, interference control, and tradeoff control between sector-accumulated throughput and cell-edge user throughput. The SMST performance gain over FPC can be more than 40%.

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Mobile Backhaul Solutions

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Abstract: In this paper, we give an overview of mobile backhaul solutions and propose an MPLS-centered solution that takes into account timing synchronization, OAM, and protection. We also propose an evolved protection bandwidth allocation mechanism that makes the transport network as efficient as possible.

Keywords: mobile backhaul; multiprotocol label switching (MPLS); optical networking; protection

1 Introduction

Recent advances in cellular technology have necessitated significant improvement in the mobile backhaul network. With increased use of smartphones and laptops, mobile communication has been moving from voice-centered infrastructure to data-centered infrastructure.

New mobile technologies, such as high-speed packet access (HSPA+) and LTE, have significantly increased downlink and uplink speeds over the radio link. Improvements over the radio access link demand similar improvement in bandwidth on the backhaul network.

However, current backhaul networks are based on legacy technologies that are optimized for voice transport. To benefit from advances in radio access link technologies, the backhaul network needs to be transformed from a slow, TDM-centered network into a high-speed, data-centered network.

Driven by bandwidth demand of the Internet, engineers have been building high-speed, data-centered networks for many years. However, building a mobile backhaul network is very different from building a commercial data network. A mobile backhaul network requires

- QoS-based traffic with strict

requirements on delay and jitter

- high availability
- timing synchronization
- frequency and phase synchronization for optimal handover
- coordinated multipoint transmission (CoMP) and interference cancellation in LTE-Advanced
- enhanced OAM
- multiple transport modes that support data traffic and TDM traffic for legacy base stations
- symmetric bandwidth requirements for the up-stream and down-stream between the central office and base stations.

In traditional wired broadband access, bandwidth is usually asymmetrical. As the use of cloud services increases, symmetrical bandwidth in both directions becomes more important when designing the network.

In this paper, an Ethernet/MPLS-based solution is proposed to satisfy mobile backhaul requirements. The solution addresses the following issues:

- Depending on the situation, the migration path from the backhaul network (based on legacy technology) to the new infrastructure (capable of supporting the new cellular technologies such as LTE) may be different.
- High availability necessitates

protection infrastructure. A means of efficiently reserving bandwidth on the protection path for an MPLS-based network needs to be articulated.

- OAM techniques of data-centered networks need to be incorporated into traditional transport networks.

- Traffic aggregation needs to be performed closer to the base stations.

In this paper, a new trend in mobile radio access network architecture is briefly discussed. In this architecture, called cloud radio access network (C-RAN), baseband processing of the radio signal is centralized. Although there are many advantages to a centralized approach in terms of power consumption and project engineering, among other things, C-RAN also requires a very different transport network between the radio amplifiers and antenna, and the central location where baseband signals are processed.

2 Basic Requirements

During mobile communication, connectivity from the base station to the central office occurs over the mobile backhaul network.

In this backhaul network, traffic for different generations of the radio access network is transported. Different generations of cellular technologies have different architectural names to indicate cell-site equipment and the

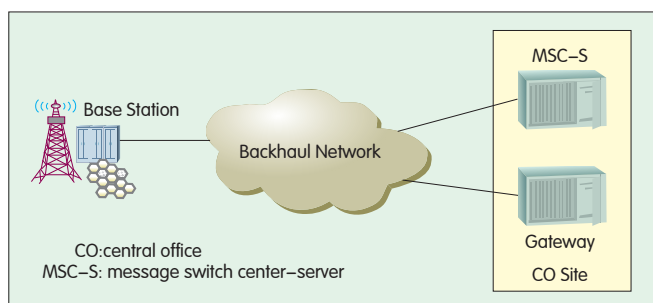


Figure 1.
Mobile backhaul network.

corresponding equipment in the central office (CO). In this paper, the cell-site equipment is called base station unless otherwise noted (e.g. in LTE, the base station is eNodeB). The central office equipment is called message switch center-server (MSC-S) for voice, and gateway for data (e.g. SAE-GW for EPC, SGSN for UTRAN). The backhaul network is shown in Fig. 1.

Connectivity between the base station and the CO site is determined by the technology used in the RAN, the location of the cell site, the bandwidth requirements, and local regulations.

In a GSM (voice and limited data traffic) and UMTS/CDMA 2000 (voice-centered with increasing data traffic) mobile network, many cell sites use microwave as backhaul technology. However, in the LTE era of wide spectrum and high data rate, the microwave-based backhaul network does not have adequate bandwidth. In this paper, we discuss a fiber-based mobile backhaul network.

The current practice for building mobile backhaul networks is a flat IP-centered architecture. To support legacy mobile technologies, one of the key requirements of a mobile backhaul network is support for a native TDM interface. Support for such an interface usually comes in the form of circuit emulation, for example, PWE3 emulation, in the flat IP network.

Different generations of mobile network also have different delay and jitter requirements. For LTE, Next Generation Mobile Network Alliance (NGMN) specifies a maximum delay of 5 ms (one way), and there are no specific jitter requirements.

The common requirement for LTE bandwidth, which also depends on spectrum width and the number of

carrier-sections, is around 300–400 Mbit/s. In LTE, the physical layer can be gigabit Ethernet, 10G Ethernet (in sharing mode), GPON, or 10G EPON.

Normal EPON is not included in the physical layer because the sharing capability of the link is a maximum of 1G. 10G GPON is also omitted because current 10G GPON has asymmetric bandwidth.

Fig. 2 shows the basic requirements for a mobile backhaul for advanced mobile technologies such as LTE and LTE-Advanced.

3 MPLS-Based Solutions

In this section, the specifics of using multiprotocol label switching (MPLS) technology for mobile backhaul application are articulated.

Apart from the final access link (which can be xPON-based), inside the mobile backhaul network, the layer-2 technology is Ethernet. With Ethernet, technologies such as Layer-2/Layer-3 virtual private network (VPN), pseudo-wire for circuit emulation in supporting TDM traffic, and MPLS can be easily supported.

For mobile backhaul applications, a pure IP-based network with no MPLS can also provide adequate service with increases in delay and jitter. These

increases are due to an increase in processing at each hop. With an IP transport network supporting multiple services, and considering IP router port cost and processing complexity, mobile backhaul can best be implemented via an MPLS-based network.

Another contender for mobile backhaul could be optical transport network (OTN) with ODU-0 to transport gigabit Ethernet signals. But an OTN network is TDM in nature and cannot be as flexibly deployed as an MPLS network.

3.1 QoS and CoS

To make the network scalable so that it can provide many different types of services, CoS is usually used with queuing and discard techniques. A mobile backhaul network needs to queue and discard priorities from the radio access network.

In almost all radio access technologies, the relative queuing and/or discard priorities are marked. After baseband processing of the radio signals at the entrance of the mobile backhaul network, the markings on the radio signals need to be remapped onto the technologies used in the backhaul network.

The core technology used in the mobile backhaul network is MPLS over Ethernet. For layer-2 (Ethernet), the 802.3p bits can indicate the priority of the packet. At the starting point of the MPLS label switched path (LSP), the EXP bits can also indicate the priority of the packet.

3.2 Timing Synchronization

In a mobile backhaul network with Ethernet and MPLS, timing needs to be synchronized for better handoff support, better voice/video quality,

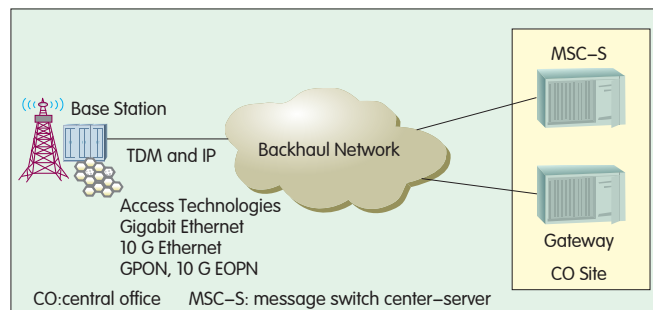


Figure 2. ▶
Mobile backhaul network
access technologies.

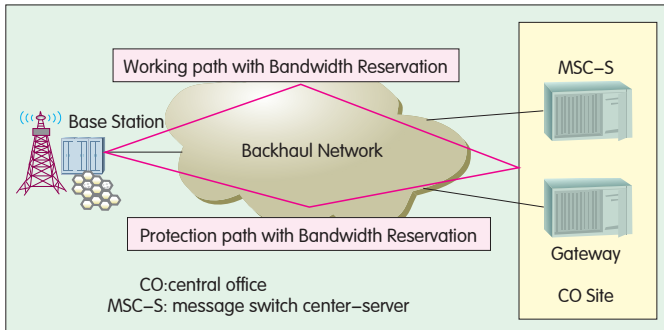


Figure 3. Protection path and bandwidth reservation in the MPLS network.

lower interference, and better bandwidth (e.g. CoMP).

There are a number of ways of supporting timing synchronization, each of which has different advantages and disadvantages:

- GPS based timing. This is accurate for frequency and can also be used for phase synchronization. The drawback is that GPS is often unavailable because of a poor environment for acquiring GPS signals or because the U.S. government has encrypted the signals.

- packet-based timing synchronization (IEEE1588v2). This synchronization mechanism has been widely evaluated over the past a few years. It is adequate for synchronization in universal mobile telecommunications system (UMTS) networks. A CDMA network uses GPS timing. The performance of this mechanism in synchronizing timing for more time-stringent requirements, such as CoMP, still requires further study.

- synchronous Ethernet. This scheme only works if Ethernet is provided end-to-end. In this case, the last access link also needs to be Ethernet, and an xPON-based solution is excluded. Synchronous Ethernet can be deployed if the carrier is not using xPON-based technologies for the access link between the backhaul network and the base station.

3.3 OAM for MPLS-Based Network

OAM is an important and fundamental in transport networks[1]. It contributes to

- reducing operational complexity and costs because it allows for efficient and automatic detection, localization, handling, and diagnosis of defects. It

also minimizes service interruptions and operational repair time.

- enhancing network availability by ensuring that defects, such as those resulting in misdirected customer traffic, are detected, diagnosed, and dealt with before a customer reports the problem.

- meeting service and performance objectives. OAM allows service-level agreements (SLAs) to be verified in a multimaintenance environment and allows service degradation caused by packet delay or packet loss to be determined.

A backhaul solution should support end-to-end OAM in a multivendor environment and simplify network operations with OAM tools.

Currently, the telecommunication standardization sector (ITU-T) SG15 and Internet engineering task force (IETF) are cooperating on MPLS transport profile (MPLS-TP). Compared with MPLS, OAM is a very important characteristic of MPLS-TP. Fault management (FM) OAM functions, such as continuity check (CC), continuity verification (CV), and remote defect indication (RDI), can automatically detect and localize defects that occur in network. Performance management (PM) OAM functions, such as packet loss measurement (LM), packet delay measurement (DM), and throughput measurement, can diagnose service degradation. OAM functionality is also the key for network survivability and

triggering network protection.

4 Protection Bandwidth Reservation

MPLS-based mobile backhaul is a mesh network with bandwidth assurance. When high availability is required, bandwidth also needs to be assured when the network experiences a limited fault, such as a single fiber cut or a single MPLS transport nodal failure.

The current method of supporting high-availability is to provide a working path and a protection path. The required bandwidth is allocated on both the working path and protection path. If the working path experiences a failure, the protection path is used. Because the bandwidth is also allocated on the protection path, bandwidth is assured for the backhaul network. This arrangement is shown in Fig. 3.

The protection bandwidth reservation scheme assures bandwidth when there is limited network failure, but shared protection between many different cell sites is not taken into account. This critical flaw is shown by the simple ring topology in Fig. 4.

In the arrangement in Fig. 4, the protection bandwidth reserved on the link between nodes 5 and 6 (same as other links) is the sum of the bandwidth for the working paths A and B. If we assume a single failure on any node and take into consideration the ring structure, the maximum bandwidth required for protection is the maximum bandwidth for working paths A and B.

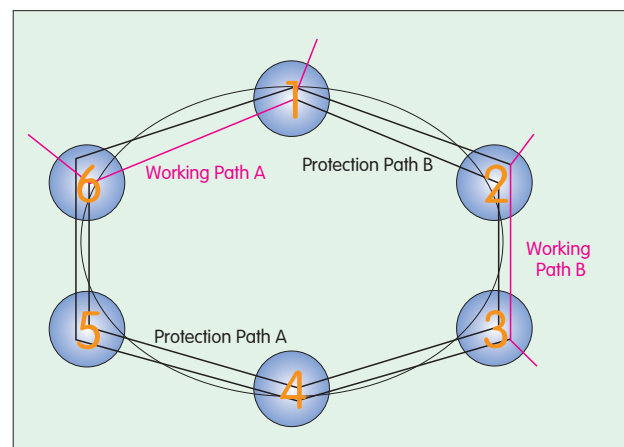


Figure 4. Current working and protection-reservation method.

Bandwidth reservation for any link is performed in the egress direction. The adjacent node is concerned with the ingress direction, which is its egress direction on the link concerned.

For bandwidth reservation in a packet network, equivalent bandwidth is usually used. For any packet stream, the equivalent bandwidth is usually derived from the peak bandwidth, average bandwidth, maximum burst size, buffer size, and packet loss probability. The equivalent bandwidth is somewhere between the average bandwidth and the peak bandwidth. The theory of equivalent bandwidth, sometimes also called effective bandwidth, is discussed in [2] and [3].

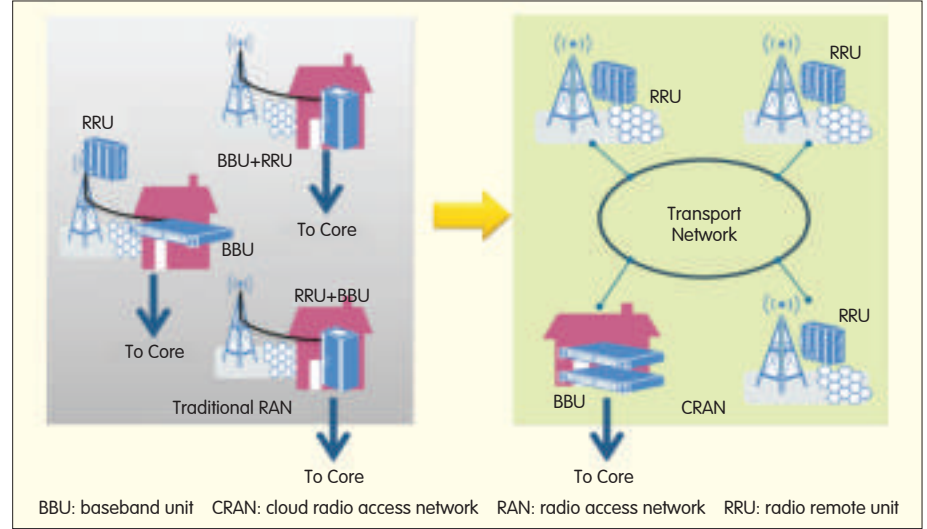
In the following, for simplicity, the bandwidth required for reservation implies the equivalent bandwidth.

A link k on node Y is given by $Y(k)$, $k = 1, \dots, K_Y$. There are K_Y links for Y . The egress bandwidth on a particular link has four main features:

1) Normal working bandwidth. This is the bandwidth required if there is no failure inside the network. For a nodal link $Y(k)$, $1 \leq k \leq K_Y$, the bandwidth, $B_N(Y(k))$ is the sum of the equivalent bandwidths of all the working paths over $Y(k)$.

2) Bandwidth may be absent on $Y(k)$ because of the failure of link i of node J (i.e. $J(i)$ failure). For any working path over $Y(k)$ and $J(i)$, when there is $J(i)$ failure, the working-path traffic is absent if the working path goes over $J(i)$ before $Y(k)$. There is a difference between 1+1 protection [4] and MPLS fast reroute protection [5]. The working path traffic is absent for 1+1 protection and may be absent for MPLS fast reroute, depending on topology and the detour path. Depending on the protection scheme, the working-path traffic may be absent if the working path goes over before $Y(k)$. In this paper, this bandwidth is $B_s(Y(k), J(i))$, where $1 \leq k \leq K_Y$ and $1 \leq i \leq K_J$.

3) Bandwidth may be absent on $Y(k)$ due to failure of J . For a complete failure of J , the bandwidth absent on link $Y(k)$ is $B_a(Y(k), J(0))$. In this case, the notation is the same as that for bandwidth absent because of link failure, and $J(0)$ denotes the nodal



▲ Figure 5. From traditional RAN to C-RAN.

failure.

4) Protection bandwidth on $Y(k)$, $1 \leq k \leq K_Y$ because of failure on $J(i)$, $0 \leq i \leq K_J$. This failure includes both link and nodal failures. In such failures, the equivalent bandwidth for the protection path is $B_p(Y(k), J(i))$, where $1 \leq k \leq K_Y$ and $0 \leq i \leq K_J$.

All the required qualities, $B_N(Y(k))$, $B_s(Y(k), J(i))$, and $B_p(Y(k), J(i))$, where $0 \leq i \leq K_J$ for any $1 \leq k \leq K_Y$, are available once the working path and the protection scheme is determined.

With this information, we are ready to define a quantity

$$P(Y(k), J(i)), Y \neq J \quad (1)$$

where $P(Y(k), J(i)) = B_p(Y(k), J(i)) - B_s(Y(k), J(i))$, and $0 \leq i \leq K_J$.

If there are N nodes in the network, for all values of J , where $1 \leq J \leq N$, $J \neq Y$, and for all values of i , where $0 \leq i \leq K_J$, a list in descending order can be constructed based on $P(Y(k), *)$ for a particular $Y(k)$, $1 \leq k \leq K_Y$. This list is given by

$$P(Y(k), J_1(i_1)), P(Y(k), J_2(i_2)), \dots, P(Y(k), J_M(i_M)) \quad (2)$$

where $M = \sum_{i=1, i \neq Y}^N K_i + N - 1$. The notation J_x is defined as $J_x \in (1, \dots, N)$, $J_x \neq Y$ and $1 \leq x \leq M$.

In the ordered list, we have

$$P(Y(k), J_1(i_1)) \geq P(Y(k), J_2(i_2)) \geq \dots \geq P(Y(k), J_M(i_M)) \quad (3)$$

For a single link or node failure in the

network, the protection bandwidth to be reserved for $Y(k)$ is $P(Y(k), J_1(i_1))$.

If the topology constraint is ignored, the upper bound for bandwidth reservation on $Y(k)$ that is necessary to handle m faults is the sum of the first m members of the ordered list. That is,

$$\sum_{k=1}^m P(Y(k), J_k(i_k)) \quad (4)$$

By using this method for reserving protection bandwidth, the mobile backhaul network is efficient and competitive. A tighter upper bound based on topology and traffic flow is also possible for multiple failures, and this will be left for future discussion.

5 New RAN Architecture: C-RAN

To this point, there has been no change to the traditional mobile network architecture, where base stations consist of the radio unit (RRU) and baseband processing unit (BBU).

The RRU and BBU are connected with fiber optics. The RRU is located with the antenna on top of the cell tower, and the BBU sits on the ground.

The BBUs for many different cell sites can be co-located to provide centralized baseband processing. The resulting architecture is called cloud radio access network (C-RAN) and is shown in Fig. 5.

Because the modulated radio signals are transported between RRU and

BBU, the requirements in terms of bandwidth, delay, and jitter are much more stringent than those in mobile backhaul networks. The preferred method of transport between the BBU and RRU are direct fiber connection or wavelength division multiplexing (WDM) if conservation of fiber links is required.

Because of fiber connectivity in advanced mobile technology, variations, such as C-RAN, on traditional RAN architecture become feasible.

C-RAN architecture is still in its infancy. Further division of the workload between BBU and RRU according to transport requirements warrants further study.

6 Conclusion

In this paper, we have reviewed mobile backhaul requirement for

current and future mobile access technologies. An MPLS-based mobile backhaul solution is proposed, and timing synchronization, MPLS OAM, and protection have been discussed. A new mechanism for reserving protection bandwidth is described. This mechanism ensures that protection bandwidth is efficiently reserved for a single fault and that an upper-bound protection bandwidth estimation mechanism is provided for multiple faults.

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The Internet of Things and Ubiquitous Intelligence (4)

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Editor's Desk:

The traditional Internet is oriented towards person-to-person connection, whereas the Internet of things (IoT) is oriented towards connections between inanimate objects. IoT covers a larger range of connections and involves more semantics than traditional Internet. Traditional Internet and telecom networks focus on information transfer, but IoT focuses on information services. By combining sensor networks, Internet, telecom networks, and cloud computing platform, IoT can sense, recognize, affect, and control the physical world. The physical world can be unified with the virtual world and human perception. In this part, we discuss cloud computing and the cyber-physical system (CPS).

services applications. It expands hardware capacity, makes software reconfiguration reduces easier, overheads of software virtual machines is reduced, and supports multiple operating systems. With virtualization, use of the server is greatly enhanced.

8.2.2 Data Storage and Management

In cloud computing, data is highly reliable and highly available because of storage redundancy. Data storage technologies involve cluster computing, data redundancy, and distributed storage.

The frequency of data access is much higher than that of data update because of one characteristic of cloud computing—analyzing the stored and accessing massive data [1]. Therefore, cloud data management focuses on optimizing the data access operation.

8 Cloud Computing

A distributed CPU is the core component in cloud computing and plays a pivotal role in the development of the Internet of things. Combining cloud computing and the IoT can boost the entire industry and value chain if capability and resource sharing, quick service deployment, expansion of new human-thing interactive services, and deep data mining are optimized. When the Internet of things reaches a certain level, its dependence on cloud computing will be greater.

8.1 Concept and Current Status

With the development of electronics, communications, computers, and network technologies, cloud computing is an inevitable stage in the evolution of turing computing to network computing. Based on the Internet, network computing provides applications with

hardware, infrastructure, platform, software, and storage services. The term “cloud” vividly describes the characteristics of cloud computing: virtualization, transparency, scalability, and elasticity. It is an apt term for describing the abstraction of underlying infrastructure.

Cloud computing integrates distributed computing, parallel computing and grid computing. At its core, it virtualizes computing, resources of large data centers and provides these to users as a service.

8.2 Key Technologies

Cloud computing is a form of data-intensive super computing. It has unique data storage and management technologies and a unique programming model.

8.2.1 Virtualization

Virtualization is at the core of cloud computing, and is the basis for all cloud

8.2.3 Parallel Programming

The cloud computing programming model must be very simple, and complicated parallel execution and task scheduling must be hidden in the background. The programming model must be transparent, enabling users to develop programs for specific purposes.

Most cloud computing systems adopt Google's MapReduce [2]. This is a distributed parallel programming model and also an efficient task-scheduling model.

8.3 Combining with the Internet of Things

Cloud computing and IoT are complementary. Development of IoT requires the powerful processing and storage capabilities of cloud computing. If cloud computing infrastructure is used to mine, process, and analyze mass data collected on the ubiquitous sensing layer, IoT can quickly, accurately, and intelligently

manage and control the physical world and provide technical support for ubiquitous services. The IoT will also be the largest user of cloud computing services, which will, in turn, lay the foundation for more successful cloud computing.

9 Cyber-Physical System

Cyber-physical system (CPS) was first proposed by the US National Science Foundation (NSF) in 2006. CPS is expected to become the third wave of information technology following the computer and the Internet. CPS ubiquitous sensing, control, and computing and the close integration of human, machines, and things are the ultimate goals of IoT.

9.1 CPS Overview

CPS is complicated a multidimensional, embedded system that is integrated with computing, network and physical environments. With the integration of 3C (computation, communication, and control) technologies, CPS delivers real-time sensing, dynamic control, and information services for large engineering systems. Through interactive, cyclic feedback in computing and physical processes, CPS closely integrates these processes and adds or expands new functions in real time. In this way, a physical entity can be monitored and controlled in a secure, reliable, efficient, and real-time manner [5].

9.2 Characteristics

CPS has the following characteristics:

- It integrates computing, communication, and control because it embeds computing capability deeply into each physical subsystem. It aims for precise control over the physical processes in networks.
- It requires the integration of computing and control technologies. To connect the cyber world to the physical world, CPS should integrate computing technologies (which are discrete event-relevant and indifferent to time and space) with the control technologies (which are continuous

process-relevant and time space-focused), enabling the discrete computing process to interact and tightly couple with the continuous physical process.

- It is adaptive to dynamic changes in the physical world; it has powerful reorganization and reconstruction capabilities; it can easily; and it is easy to connect with other CPS subsystems.

- Because it has multidimensional time-space complexity, CPS should be an open, trustable, and predictable embedded system. The embedded computing system of CPS interconnects and interoperates with other cyber systems via the Internet. Furthermore, CPS has stepped into fields that are closely related to national infrastructure and people's daily lives. It is sensitive to security, and its technologies and products must be precise and highly reliable.

9.3 Challenges

To realize the goals of CPS, there are some technical challenges to be addressed. A good architecture is critical in maintaining scalability, durability, diversity and continuous technical innovation in CPS [3]. It is also the key to customer investment.

To ensure sustainable development of CPS, the architecture should be stable, a clear roadmap should be devised that can lead to a targeted study based on core CPS architecture, and a development schedule should be in place so that technical achievements are planned and predicted. The natural development cycle should be balanced.

There are several challenges in the development of CPS. The theoretical basis differs from the application model. The key to the success of a technology is its deployment in actual environments. It is also necessary to maintain the integrity, reliability and security of the architecture. Because of uncertainty in the external environment and potential changes, CPS should respond to a system failure or malicious attack automatically, autonomously, and quickly. According to the characteristics described in 9.2 the OS and architecture should be able to manage redundant resources on the

interconnected device layers, monitor errors in user applications and physical components, and quickly recover CPS from a system failure. Electricity CPS is a critical infrastructure, and guaranteeing its security is an important issue.

10 Summary

The IoT, cloud computing, and CPS interact and couple with each other. IoT is the intuitive application of CPS, and cloud computing provides technical support for IoT information service. The demands of economy and society on the Internet of things and CPS go far beyond existing applications. Therefore, from the perspective of economic development and technical innovation, IoT and CPS are a trend in the development of global information technologies and industry. They will have a profound effect on existing industrial structure, become the core competence in the new industrial structure, and cultivate new economic growth.

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