



An Improved Parasitic Parameter Extraction Method for InP HEMT

Abstract: An improved parasitic parameter extraction method for InP high electron mobility transistor (HEMT) is presented. Parasitic parameter extraction is the first step of model parameter extraction and its accuracy has a great impact on the subsequent internal parameter extraction. It is necessary to accurately determine and effectively eliminate the parasitic effect, so as to avoid the error propagation to the internal circuit parameters. In this paper, in order to obtain higher accuracy of parasitic parameters, parasitic parameters are extracted based on traditional analytical method and optimization algorithm to obtain the best parasitic parameters. The validity of the proposed parasitic parameter extraction method is verified with excellent agreement between the measured and modeled S-parameters up to 40 GHz for InP HEMT. In 0.1 – 40 GHz InP HEMT, the average relative error of the optimization algorithm is about 9% higher than that of the analysis method, which verifies the validity of the parasitic parameter extraction method. The extraction of parasitic parameters not only provides a foundation for the high-precision extraction of small signal intrinsic parameters of HEMT devices, but also lays a foundation for the high-precision extraction of equivalent circuit model parameters of large signal and noise signals of HEMT devices.

Keywords: parasitic parameters; open-short test structure; parameter extraction; HEMT

DUAN Lanyan¹, LU Hongliang²,
QI Junjun², ZHANG Yuming²,
ZHANG Yimen²

(1. ZTE Corporation, Shenzhen 518057, China;
2. Key Laboratory of Wide Band-Gap
Semiconductor Materials and Devices, Xidian
University, Xi'an 710071, China)

DOI: 10.12142/ZTECOM.2022S1001

<http://kns.cnki.net/kcms/detail/34.1294.TN.20220119.1715.004.html>, published online
January 20, 2022

Manuscript received: 2021-05-16

Citation (IEEE Format): L. Y. Duan, H. L. Lu, J. J. Qi, et al., "An improved parasitic parameters extraction method for InP HEMT," *ZTE Communications*, vol. 20, no. S1, pp. 01 – 06, Jan. 2022. doi: 10.12142/ZTECOM.2022S1001.

1 Introduction

Compared to traditional Si-based Complementary Metal Oxide Semiconductor (CMOS) devices, InP high electron mobility transistors (HEMT) have better frequency response characteristics, power density and breakdown voltage, which makes InP HEMT an excellent candidate for many monolithic microwave integrated circuits (MMICs) working at gigahertz frequency ranges^[1-2]. As an important link between transistors and circuits, a small signal model is the basis of all device models. Therefore, the model accuracy depends mostly on the small signal equivalent circuit model which can reflect the physical and electrical properties of the device^[3].

The extraction of parasitic parameters is the first step of small signal model parameter extraction and its accuracy has a great influence on the subsequent extraction of intrinsic pa-

rameters. Commonly used parasitic parameter extraction methods include the open-short test structure method and cold-field effect transistor (FET) method. The former^[4-6] requires a test structure with the same size as the pad on a chip. The latter uses the equivalent circuit model of an HEMT device under the pinch off condition to extract parasitic parameters. The gate voltage is set at the threshold voltage and the drain source bias is set to zero. In Ref. [7], two identical capacitors C_b are used to simulate gate-to-source and gate-to-drain depletion layer capacitances. C_{pd} depends on the channel capacitance. A large C_b will cause a larger value of C_{pd} , and C_{pd} will be obviously overestimated. In order to avoid C_{pd} being overestimated, WHITE et al.^[8] added the third capacitance based on the Dambrin method, which is equal to C_b . The final results show that this method tends to underestimate C_{pd} . All cold-FET methods are based on the assumption that C_{gs} and C_{gd} of symmetrical field effect devices are equal under cold-FET bias. For the general HEMT device, this assumption is obviously not true.

Aiming at the problems of traditional methods, a new meth-

This work was supported by ZTE Industry–University–Institute Cooperation Funds under Grant No. HC-CN-20191121016.

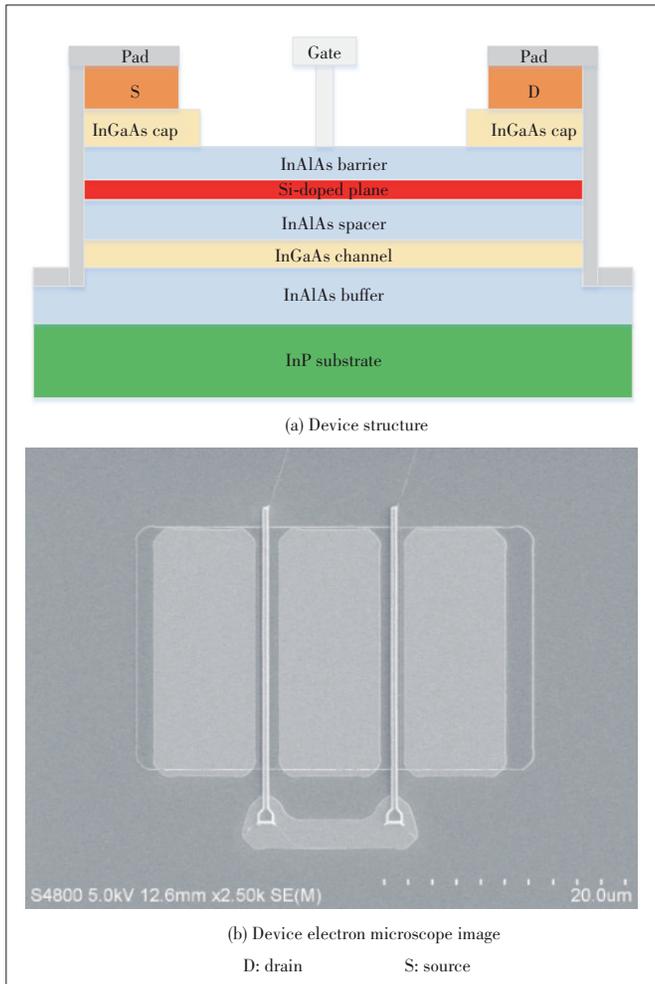
od combining analytical and optimization methods to extract parasitic capacitance and inductance is proposed in this paper. Compared with previous literatures^[7-8], the proposed method has high accuracy and no complicated extraction process. Firstly, parasitic parameters obtained by the analytical method are used as the initial values of the optimization method, then the optimization method is used to optimize and fit the parasitic parameters, and finally the optimal values are obtained. The high precision of the values obtained by the proposed method has been validated by the open-short test structure method.

2 Device Structure and Model Description

Fig. 1 shows the structure and electron micrographs of an InP HEMT device. The substrate is a semi-insulating InP substrate, and the buffer layer uses $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ material with a small lattice mismatch with the InP substrate, which is mainly used as a connecting liner. The bottom and the functional layer can prevent impurities from the substrate entering the chan-

nel. The channel layer uses a narrow band gap $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ material, and the barrier layer uses an n-type doped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ material. The channel and barrier layers will generate two-dimensional electron gas. The band is narrow, so the two-dimensional electron gas will be stored in the potential well at the interface of the channel layer to form a conductive channel. In order to reduce the Coulomb scattering of the channel two-dimensional electron gas by the barrier layer impurities, a thin layer of intrinsic $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ is added between the channel layer and the barrier layer. The cap layer uses a highly doped narrow band gap InGaAs material, which aims to form a good ohmic contact while reducing the source and drain resistance. A T-shaped gate is used to reduce the gate length and improves frequency characteristics while avoiding the increase of gate parasitic resistance, so that the device has better frequency characteristics.

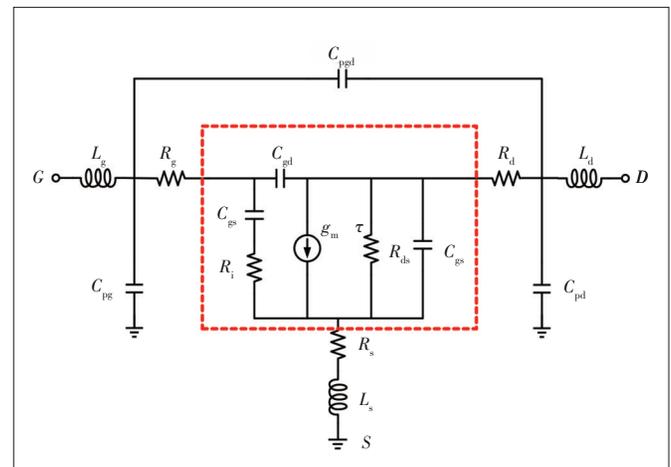
Fig. 2 shows the small signal equivalent circuit topology for this device. This equivalent circuit includes two parts: the inner part contains intrinsic elements and the outer part contains parasitic elements. L_g , L_s and L_d represent the gate, source and drain pad parasitic inductances; R_s and R_d are the source and drain parasitic resistances, and R_g is the gate distributed resistance; C_{pg} , C_{pgd} and C_{pd} are the gate and drain pad parasitic capacitances; C_{gs} , C_{gd} and C_{ds} represent the gate-source, gate-drain, and drain source capacitances, respectively; R_i , R_{gd} and R_{ds} are the charge and output resistances; τ and g_m are the intrinsic delay and intrinsic transconductance, correspondingly. C_{gs} , C_{gd} , C_{ds} , R_i , R_{gd} , R_{ds} , τ and g_m are intrinsic elements which are emphasized by the red dashed frame in Fig. 2. The rest are extrinsic elements which are considered to be bias independent.



▲ Figure 1. Photograph of InP high electron mobility transistor (HEMT) device structure

3 Extrinsic Model Parameter Extraction and Verification

This modeling and circuit design uses the 0.15 μm InP



▲ Figure 2. Small signal equivalent circuit for InP high electron mobility transistors (HEMT)

HEMT process of the Institute of Microelectronics of the Chinese Academy of Sciences, with a gate width of $2 \times 20 \mu\text{m}$. The frequency range of on-wafer S -parameters is from 0.1 to 40 GHz with steps of 0.1 GHz, including an open-short test structure. The whole parasitic parameter extraction process is shown in Fig. 3.

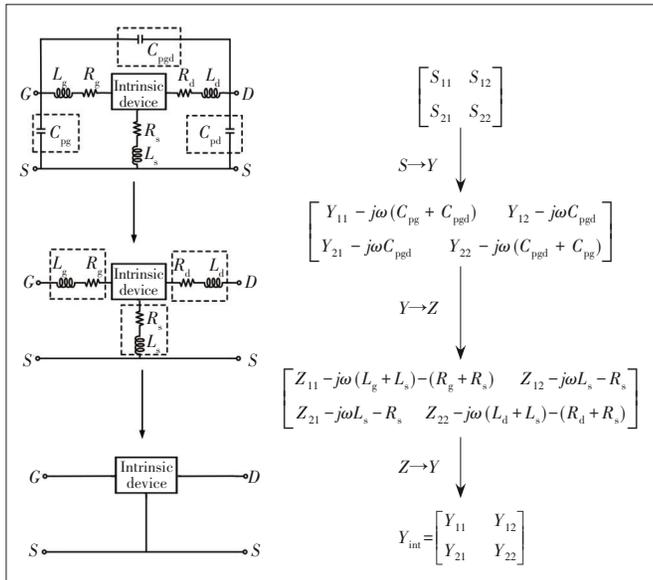
3.1 Parasitic Capacitances

The equivalent topology of dummy open structure^[9] is shown in Fig. 4. This structure can be equivalent to a π -type network, and the parameter Y can be used to solve the parasitic capacitances.

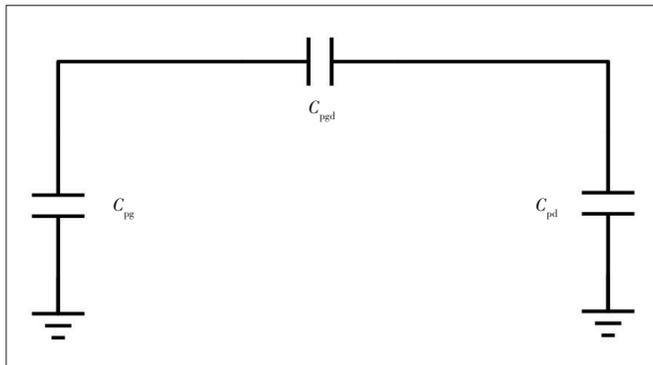
The parasitic capacitance values can be analyzed and characterized by the following formulas:

$$C_{pg} = \frac{1}{\omega} \text{Im}(Y_{11} + Y_{12}), \quad (1)$$

$$C_{pgd} = -\frac{1}{\omega} \text{Im}(Y_{12}), \quad (2)$$



▲ Figure 3. Parasitic parameter extraction process



▲ Figure 4. Equivalent circuit of the open dummy structure

$$C_{pd} = \frac{1}{\omega} \text{Im}(Y_{22} + Y_{12}). \quad (3)$$

According to Eqs. (1 – 3), three capacitance values can be extracted, as shown in Table 1.

3.2 Parasitic Inductances and Resistances

The equivalent topology of dummy short structure^[10–11] is shown in Fig. 5. This structure can be equivalent to a T-type network, and parasitic resistors and inductors in series can be extracted by the Z -parameters after the parasitic capacitances are de-embedded.

The Z -parameters of the equivalent circuit in Fig. 5 are written as

$$Z_{11} = R_g + R_s + j\omega(L_g + L_s), \quad (4)$$

$$Z_{12} = Z_{21} = R_s + j\omega L_s, \quad (5)$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s). \quad (6)$$

Usually, the parasitic inductances and resistances can be analyzed and characterized by the following formulas:

$$L_g = \frac{1}{\omega} \text{Im}(Z_{11} - Z_{12}), \quad (7)$$

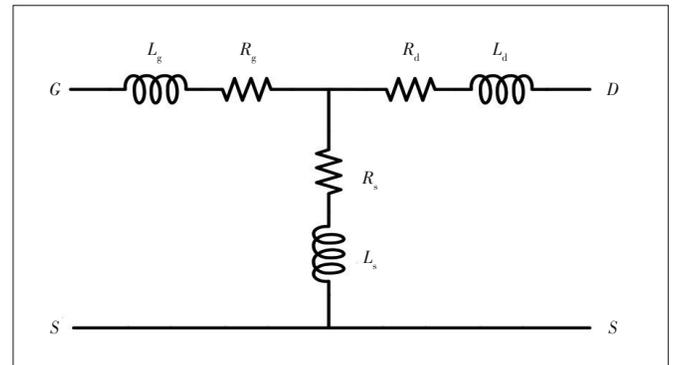
$$L_s = \frac{1}{\omega} \text{Im}(Z_{12}), \quad (8)$$

$$L_d = \frac{1}{\omega} \text{Im}(Z_{22} - Z_{12}), \quad (9)$$

$$R_g = \text{Re}(Z_{11} - Z_{12}), \quad (10)$$

▼ Table 1. Extraction of parasitic capacitance values

C_{pg} /fF	C_{pgd} /fF	C_{pd} /fF
21.497	1.647	20.407



▲ Figure 5. Equivalent circuit of the dummy short structure

$$R_s = \text{Re}(Z_{12}), \tag{11}$$

$$R_d = \text{Re}(Z_{22} - Z_{12}). \tag{12}$$

According to Eqs. (7 - 12), three inductance and resistance values can be extracted, as shown in Table 2.

Fig. 6 shows the simulation results of the extracted parasitic parameter values by dummy short structure and measurement data.

It can be found from Fig. 6 that the parasitic parameters extracted by the short structure that directly uses the Z parameters are not accurate. According to Eqs. (4 - 6), the extraction accuracy of R_s and L_s will directly affect the extraction accuracy of R_g, L_g, R_d and L_d . Fig. 6(c) shows that the real part of Z_{12} is a quantity that varies with frequency. In this case, extract-

ing R_s and L_s will increase the extraction error and further reduce the accuracy of extracting other parasitic parameters, which will lead to unsatisfactory fitting results.

There is a Chinese literature that proposed an algorithm based on feature points to simultaneously extract parasitic inductances and parasitic resistances. The author regards the three resistance and inductance series as three separate parameters, corresponding to Y_g, Y_s, Y_d , namely

$$Y_i = \frac{I}{R_i + j\omega L_i} = \frac{R_i}{R_i^2 + \omega^2 L_i^2} - j \frac{\omega L_i}{R_i^2 + \omega^2 L_i^2} \tag{13}$$

$(i = g, s, d).$

The imaginary part is

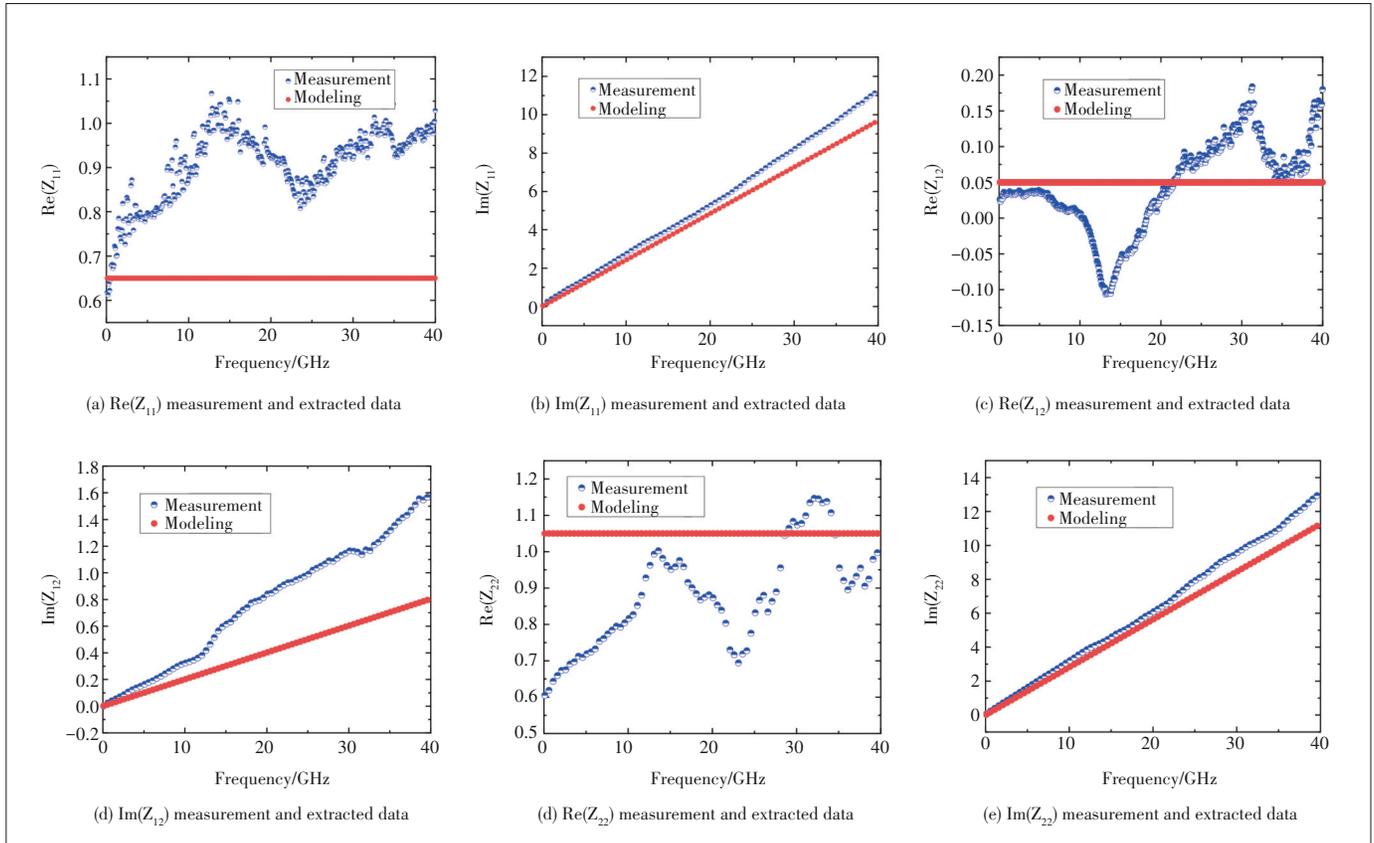
$$\text{imag}(Y_i) = -\frac{L_i}{\frac{R_i^2}{\omega} + \omega L_i^2} \quad (i = g, s, d) \tag{14}$$

From Eqs. (13) and (14), we can see that when $\omega=R/L$, $\text{imag}(Y_i)$ has a minimum value: $-1/(2R)$. Through this point, the inductance and resistance values can be extracted at the same time. The experiments show that the results of this extraction are not unsatisfactory.

Through the comparison of the research results, the open-

▼Table 2. Extraction of parasitic inductance and resistance values

Parasitic Parameter	Value
L_g/pH	35.355
L_s/pH	3.200
L_d/pH	41.599
R_g/Ω	0.600
R_s/Ω	0.050
R_d/Ω	1.000



▲Figure 6. Comparison of parasitic parameters extracted by the dummy short structure and measurement data

short structure combined with the analytical method to solve the parasitic parameters does not get satisfactory results. Based on the open-short structure, we propose a method combining analytical and optimization methods to extract parasitic parameters. We use the parasitic parameter values obtained by the analytical method as the initial values of the optimization method, and then use the optimization method to optimize the parasitic parameters to obtain the final values.

3.3 Extrinsic Parameters Verification

The extraction results of parasitic inductance and parasitic resistance obtained by the combination of the analytical method and optimization method are shown in Table 3.

Fig. 7 shows the comparison between the measured data and the modeled data of the optimization method and analytical method.

▼ **Table 3. Extraction of extrinsic inductances and resistances**

Extrinsic Parameter	Value
L_g/pH	39.467
L_s/pH	5.076
L_d/pH	47.676
R_g/Ω	0.725
R_s/Ω	0.034
R_d/Ω	0.639

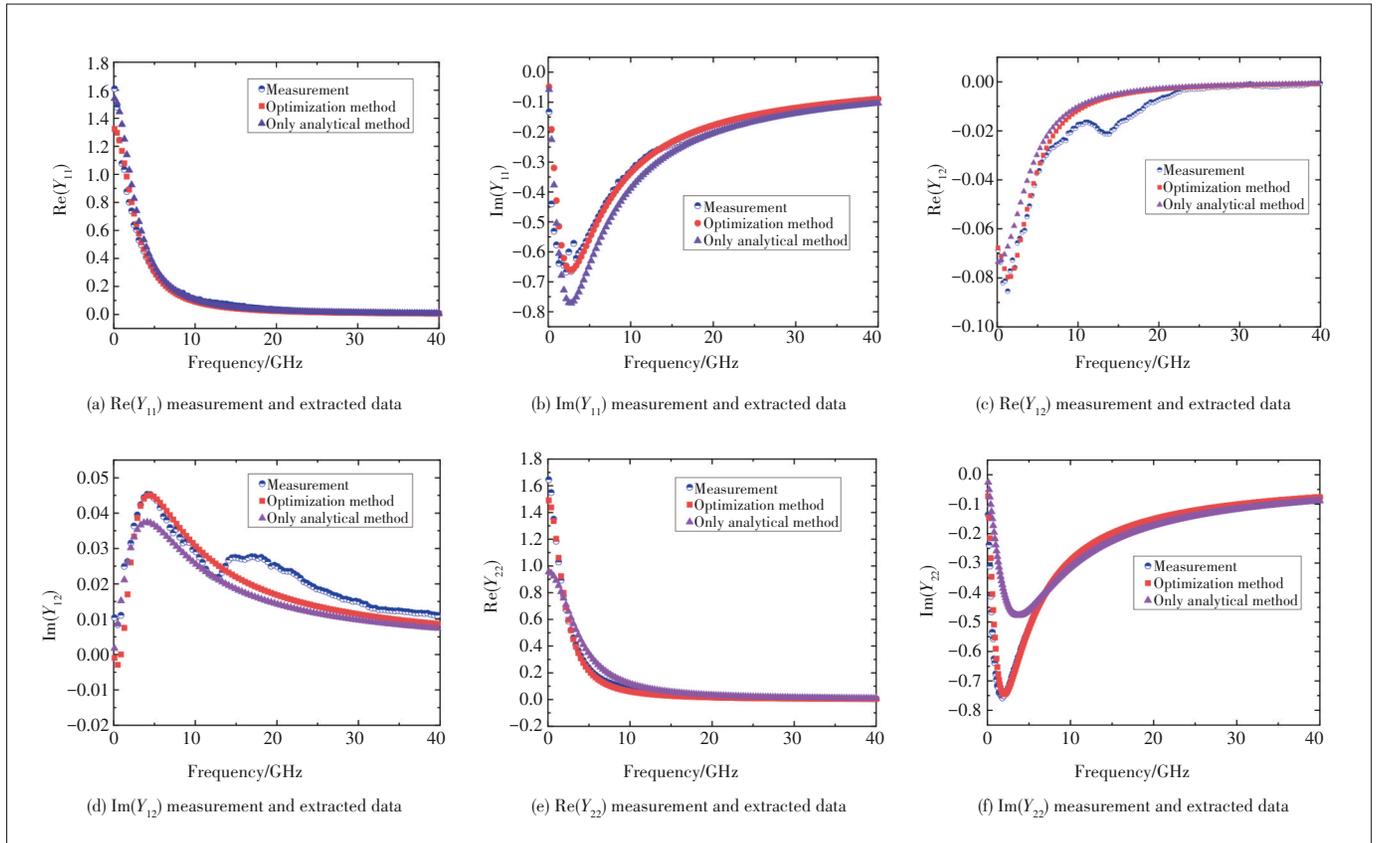
It can be seen from Fig. 7 that the parasitic parameter extraction results obtained by combining the analytical method and the optimization method fit more accurately. To further evaluate the accuracy of S -parameters, the percentage error expression, $\text{Error}(S)$, is defined as follow:

$$\text{Error}(S) = \sum_{i,j=1,2} \frac{|S_{S,ij} - S_{M,ij}|}{0.5 \times |S_{S,ij} + S_{M,ij}|} \Bigg/ 4, \quad (15)$$

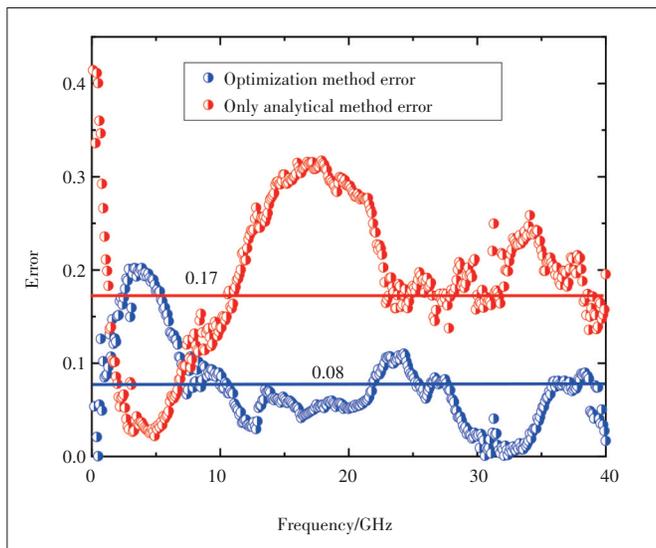
where $S_{S,ij}$ is the simulated S -parameters and $S_{M,ij}$ is the measured data. According to Eq. (15), the errors of the fitting data obtained by the two methods are calculated respectively. Comparing the error calculation results, the average relative error of the final optimization algorithm is about 9% higher than that of the analytical method (blue line in Fig. 8). In Fig. 8, the blue and red solid lines represent the average relative errors of the optimization method and the analytical method respectively, and the blue circle and red circle represent the relative errors of the optimization method and the analytical method in the whole frequency band respectively.

4 Conclusions

In this paper, an improved parasitic parameter extraction



▲ **Figure 7. Comparison of extracted parasitic parameters by dummy short structure and measurement data**



▲ Figure 8. S-parameters fitting errors of the improved extracted method

method for InP HEMT is presented. Based on the open-short structure, we use the analytical method to obtain the parasitic parameters, and then optimize the parasitic parameters by the optimization method to obtain the final values. An excellent agreement between the measured and modeled S-parameters is up to 40 GHz, which verifies the applicability of the proposed modeling methods for InP HEMT.

References

[1] KULATUNGA T, BELOSTOTSKI L, HASLETT J W. 400-to-800-MHz GaAs pHEMT-based wideband LNA for radio-astronomy antenna-array feed [J]. IEEE microwave and wireless components letters, 2018, 28(10): 909 - 911. DOI: 10.1109/LMWC.2018.2864880

[2] ALIZADEH A, MEDI A. A broadband integrated class-J power amplifier in GaAs pHEMT technology [J]. IEEE transactions on microwave theory and techniques, 2016, 64(6): 1822 - 1830. DOI: 10.1109/TMTT.2016.2552167

[3] BERRÖTH M, BOSCH R. High-frequency equivalent circuit of GaAs FETs for large-signal applications [J]. IEEE transactions on microwave theory and techniques, 1991, 39(2): 224 - 229. DOI: 10.1109/22.102964

[4] ZHONG Y H, LI K K, LI M K, et al. An improved 16-element small-signal model for InP-based HEMTs [J]. Journal of infrared and millimeter waves, 2018, 37(2): 163 - 167. DOI:10.11972/j.issn.1001-9014.2018.02.006

[5] GAO J J. RF and microwave modeling and measurement techniques for field effect transistors [M]. Raleigh, USA: SciTech Publishing Inc, 2010

[6] COSTA D, LIU W U, HARRIS J S. Direct extraction of the AlGaAs/GaAs het-

erojunction bipolar transistor small-signal equivalent circuit [J]. IEEE transactions on electron devices, 1991, 38(9): 2018 - 2024. DOI: 10.1109/16.83724

[7] DAMBRINE G, CAPPY A, HELIODORE F, et al. A new method for determining the FET small-signal equivalent circuit [J]. IEEE transactions on microwave theory and techniques, 1988, 36(7): 1151 - 1159. DOI: 10.1109/22.3650

[8] WHITE P M, HEALY R M. Improved equivalent circuit for determination of MESFET and HEMT parasitic capacitances from "Coldfet" measurements [J]. IEEE microwave and guided wave letters, 1993, 3(12): 453 - 454. DOI: 10.1109/75.251398

[9] ZHANG H S, MA P J, LU Y, et al. Extraction method for parasitic capacitances and inductances of HEMT models [J]. Solid-state electronics, 2017, 129: 108 - 113. DOI: 10.1016/j.sse.2016.12.003

[10] KAUSHIK P K, GOYAL U. Extraction and de-embedding of S-parameters using small-signal modeling for AlGaIn/GaN HEMTs [C]//14th IEEE India Council International Conference. IEEE, 2017: 1 - 6. DOI: 10.1109/INDICON.2017.8488156

[11] CHUMBES E M, SCHREMER A T, SMART J A, et al. AlGaIn/GaN high electron mobility transistors on Si(111) substrates [J]. IEEE transactions on electron devices, 2001, 48(3): 420 - 426. DOI: 10.1109/16.906430

Biographies

DUAN Lanyan received the M.S degree in circuit and system from Hunan University, China in 2002. She joined ZTE Corporation in 2002. Now, she is a senior technology and quality engineer in ZTE Corporation. Her main research direction is the development of RF material.

LU Hongliang (hllv@mail.xidian.edu.cn) received the M.S. and Ph.D. degrees in microelectronics engineering from Xidian University, China in 2003 and 2007, respectively. Since 2010, she has been a professor with the School of Microelectronics, Xidian University. Her current research interests include modeling and experiments on SiC MESFET and other devices.

QI Junjun is currently pursuing the Ph.D. degree at the School of Microelectronics, Xidian University, China. Her current research interests include model analysis and extraction of small signal equivalent parameters.

ZHANG Yuming received the M.S. degree from Xidian University, China in 1992, and the Ph.D. degree from Xi'an Jiaotong University, China in 1998. Since 2001, he has been a professor with the Microelectronics Institute, Xidian University. His current research interests include design, modeling, fabrication, and electrical characterization of SiC electronic devices for high-temperature and high-power operation. He is a senior member of IEEE.

ZHANG Yimen is a professor with the School of Microelectronics, Xidian University, China. He has also been a visiting scholar with Arizona State University, USA and a senior visiting scholar with Yale University, USA. His current research interests include wideband semiconductor devices, semiconductor devices modeling, TCAD for VLSI, and quantum well devices.