Integrated 3D Fan-out Package of RF Microsystem and Antenna for 5G Communications

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Abstract: A 3D fan-out packaging method for the integration of 5G communication RF microsystem and antenna is studied. First of all, through the double-sided wiring technology on the glass wafer, the fabrication of 5G antenna array is realized. Then the low power devices such as through silicon via (TSV) transfer chips, filters and antenna tuners are flip-welded on the glass wafer, and the glass wafer is reformed into a wafer permanently bonded with glass and resin by the injection molding process with resin material. Finally, the thinning resin surface leaks out of the TSV transfer chip, the rewiring is carried out on the resin surface, and then the power amplifier, low-noise amplifier, power management and other devices are flip-welded on the resin wafer surface. A ball grid array (BGA) is implanted to form the final package. The loss of the RF transmission line is measured by using the RF millimeter wave probe table. The results show that the RF transmission loss from the chip end to the antenna end in the fan-out package is very small, and it is only 0.26 dB/mm when working in 60 GHz. A slot coupling antenna is designed on the glass wafer. The antenna can operate at 60 GHz and the maximum gain can reach 6 dB within the working bandwidth. This demonstration successfully provides a feasible solution for the 3D fan-out integration of RF microsystem and antenna in 5G communications.

Keywords: AiP; fan-out package; RF microsystem; 3D integration; 5G communications

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1 Introduction

Owing to the growing operating frequency up to hundreds of gigahertz, minimized size and power consumption, as well as the requirement of better performance of RF system, the novel communication and sensing applications such as 5G and automotive applications are urged to integrate every section part of RF system chain, so as to establish the "everything in one" module with minisize and multi-functions. As the wave length of microwave shrinks with the growing of its frequency, the characteristically electrical length of antennas and transmitting lines can be reduced to millimeter or even micron level, which calls for higher fabrication accuracy of interconnection process. Besides, packaging process with heterogeneous integration ability offers an opportunity for novel package architecture with chips of different materials and fab features[1]. The antenna-in-package (AiP) based on wafer level fabrication process can fabricate tremendous modules simultaneously with semiconductor process, which offers compact and low cost solution and paves a possible way for RF modules with high perfor-

mance and low cost[2].

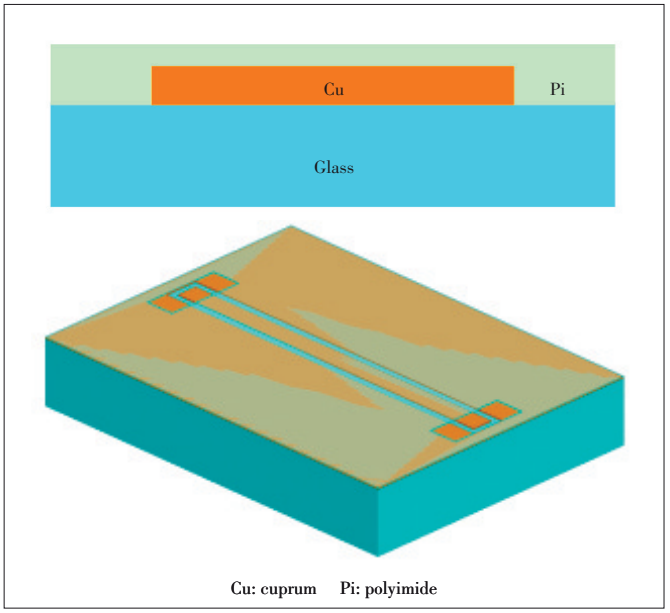
In order to meet the needs of 5G miniaturized communication systems, new packaging technologies in the millimeter wave frequency range are needed to solve the basic technical challenges of millimeter wave, such as low loss and ultra wideband interconnection, high wiring density, thin packaging substrate, high performance integrated passive devices (IPD) and reducing shape factors[3]. Dozens of papers are reported on AiP and its applications[4]. The cutting edge system corporations and outsourced semiconductor assembly and tests (OSATs) have offered numbers of AiP solutions, many of which are based on wafer level fan-out (WLFO) process, and the substrate options focus on silicon, organic compound, glass and more[5 - 6]. The glass substrate with low epsilon and coefficient of thermal expansion (CTE) is an ideal choice for high frequency application, and the compound substrate allows process flows with low price and agile combination, which is convenient for heterogeneous integration[7 - 8]. By combing glass and compound substrates in AiP module, the advantages of performance and cost can be taken together. The encapsulated antenna in 60 GHz band is a research hotspot. The traditional printed circuit board (PCB) technology is very convenient to realize multi-layer structure and antenna array[9]. The low temperature co-fired ceramic (LTCC) technology has the advantages of light and thin structure, many wiring layers and narrow line width, but its lamination temperature is higher than 850 ℃, which is much higher than that of destroying active devices. Therefore, although it is possible to create sealed multilayer substrates with integrated passive components and antennas, active devices must be packaged and connected separately because of the high temperature process of LTCC[10 - 11].

A 3D fan-out integrated packaging method for 5G communications RF microsystem and antenna is presented in this paper. Based on a new 3D fan-out wafer-level packaging architecture, the permanent bonding process of glass wafer and resin reconstructed wafer is designed. Based on glass and resin composite materials, the high density integrated interconnection of heterogeneous chip and antenna array is realized. Finally, the process manufacturing of antenna and packaging module is completed, and the high quality 5G communications AiP module manufacturing is realized. It can provide 64 antenna channels and 7 RF chips. The volume is only 18 mm × 18 mm × 1 mm, which can meet the application requirements of miniaturized 5G communications equipment.

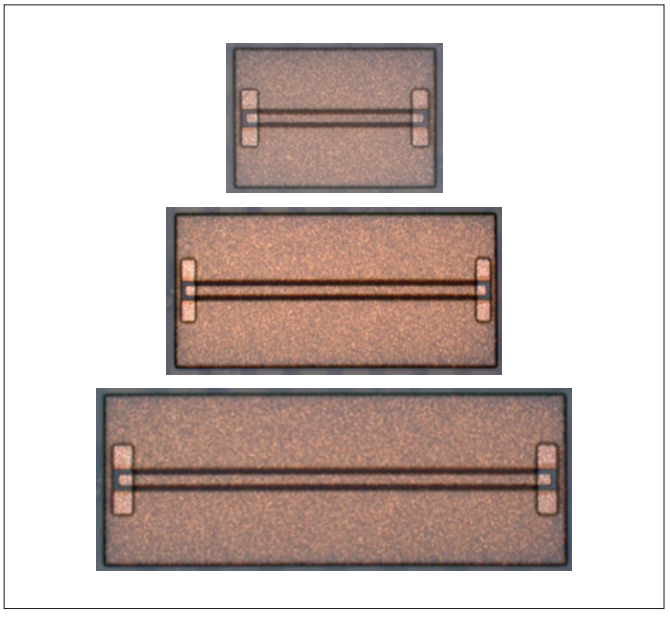
2 Measurement of Transmission Loss

In order to obtain the RF transmission performance of the 3D fan-out integrated package, a planar coplanar waveguide (CPW) transmission line and a 3D stacked CPW transmission structure are fabricated. Because the connection between the RF microsystem and the antenna usually uses CPW, it is very important to obtain the RF transmission loss of CPW[12]. The CPW transmission line is realized by redistribution layer (RDL) process in 3D fan-out wafer level packaging. The structure of CPW transmission line is distributed on both sides of the signal line, so it is very suitable for millimeter wave probe station, and more convenient for testing. The structure of CPW is shown in **Fig. 1**.

Firstly, the CPW transmission line structure is fabricated on the glass wafer. The picture of the CPW transmission line is shown in **Fig. 2**. The dielectric constant of the glass wafer is 6.3 and the dielectric loss tangent is 0.01, and the thickness of the glass substrate is 300 μm. The transmission line is made of copper and is 5 μm thick. The surface of the transmis-



▲**Figure 1. Structure of coplanar waveguide (CPW).**

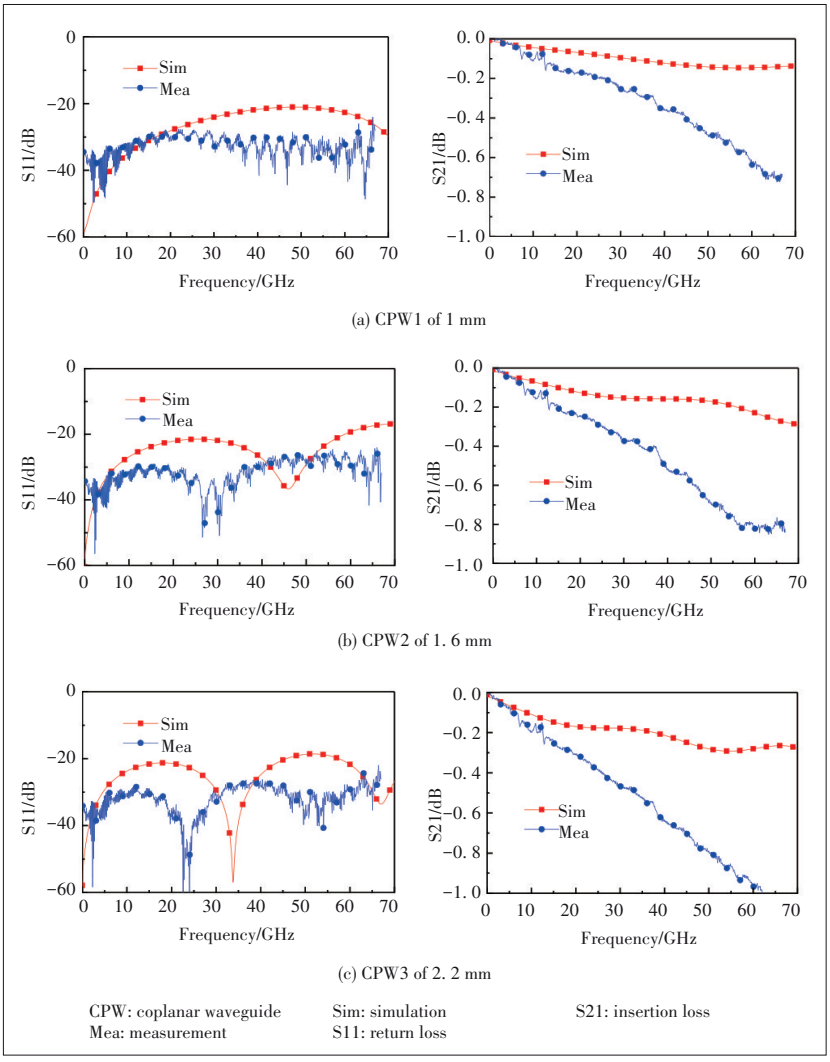


▲**Figure 2. Coplanar waveguide (CPW) with 3 different lengths.**

sion line is covered with a 10 μm thick polyimide to protect the copper wiring layer from oxidation. The width of the CPW transmission line is 70 μm and the spacing is 25 μm. CPW transmission lines with lengths of 1.00 mm, 1.60 mm and 2.20 mm are fabricated respectively. A rectangular test window of 100 μm × 300 μm is opened in the polyimide layer at both ends of the transmission line.

The transmission line is measured on a high frequency probe test bench, using a ground-signal-ground (GSG) probe with a distance of 100 μm and a phasor network analyzer (PNA) network analyzer for 67 GHz performance. The test results are shown in **Fig. 3**, and it can be found that the radio frequency transmission loss of the CPW transmission line on the glass wafer is very small. It can be seen from the figure that there are some differences between the test results and the simulation results. This is because wafer manufacturers can only give the dielectric constant and loss tangent angle of glass below 5 GHz, which makes the simulation results in the high frequency part above 5 GHz inaccurate. In addition, the test joint of the high frequency probe table will also lead to part of the insertion loss.

The transmission loss of CPW working in 60 GHz is calculated. When the CPW transmission line works in 60 GHz, the insertion loss is 0.26 dB/mm, as shown in **Table 1**, where the RF transmission loss of glass wafers is very small, and it is a good choice for 3D fan-out integration of RF microsystems and antennas.



▲**Figure 3. Comparison of test and simulation results of CPW.**

Then the glass-based CPW transmission line is packaged through the fan-out type to form a fan-out package to simulate the fan-out package structure of the RF chip. Solder balls are planted at the leading end of the package and flip-flopped on the glass-based CPW substrate to test a completed transmission link from the chip end to the package. The photos of the process structure and processing are shown in **Fig. 4**. **Fig. 5** shows the complete signal path, and the processing size of the stack interconnected package is 5 mm × 6 mm × 0.92 mm.

The 3D stacked transmission structure is finally measured in the high-frequency probe table, and the test results are shown in **Fig. 6**. It can be seen that the RF transmission loss of the 3D stacked CPW transmission structure is very small, which indicates that the 3D fan-out package structure will not bring about too much loss. Fig.6 shows that there are some differences between the test results and the simulation results. This is because the wafer manufacturer cannot give the material electrical parameters in the high frequency stage, which will affect the simulation results in the high frequency band. But the test results are basically consistent with the simulation results, which shows that the early simulation has a certain guiding significance.

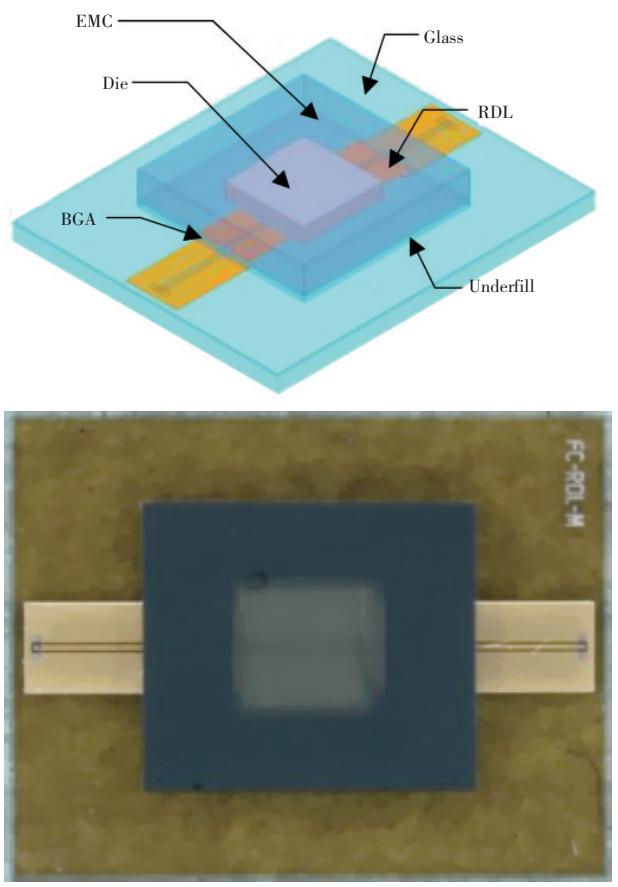
▼**Table 1. CPW transmission loss operating in 60 GHz**

Serial Number	Length/mm	Insertion Loss/dB (in 60 GHz)	Unit Length Loss (dB/mm)
CPW1	1.00	0.61	0.3
CPW2	1.60	0.79	0.23
CPW3	2.20	0.93	0.26

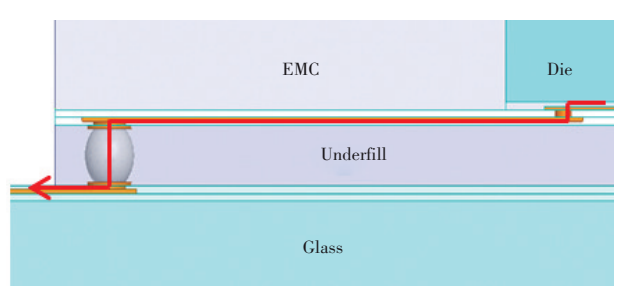
CPW: coplanar waveguide

3 Design and Measurement of AiP

The patch antenna is very suitable for wafer-level processing[13]. The wiring process is carried out on the positive and negative sides of the glass wafer (300 μm thick, dielectric constant is 6.3, and dielectric loss tangent is 0.01) to form a slot

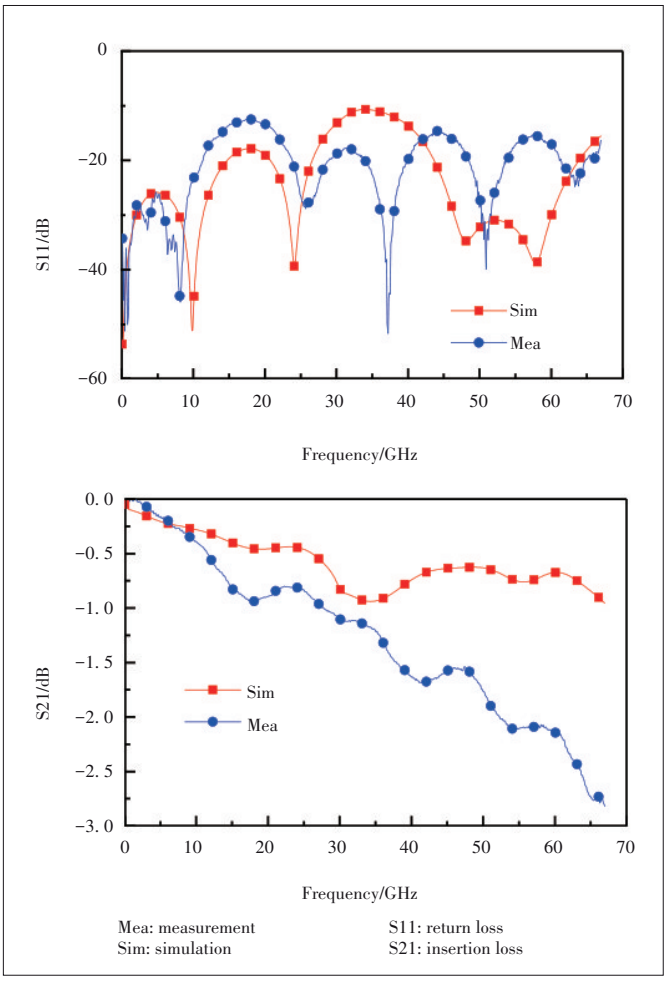


▲ **Figure 4. 3D stacked coplanar waveguide (CPW) transfer structure and photos.**



▲ **Figure 5. Transmission path of the RF signal through the package.**

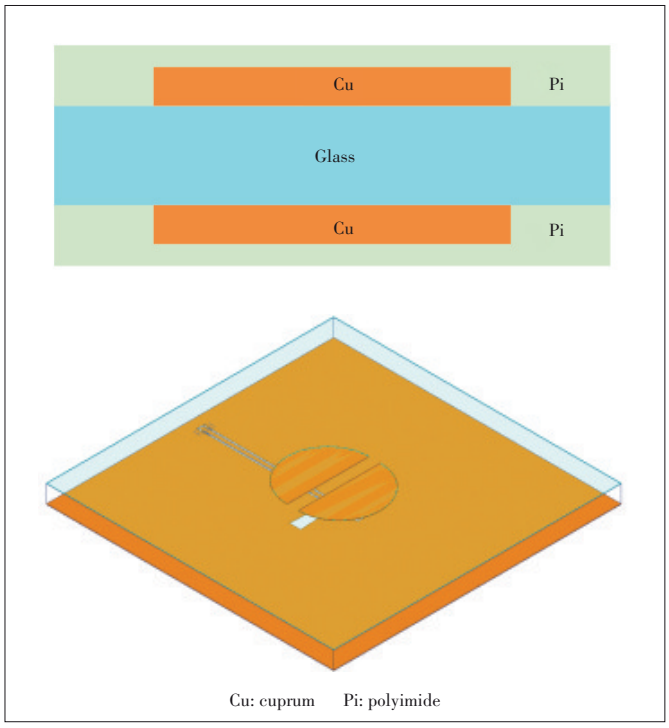
coupling antenna. The glass wafer is used as the radiation patch of the antenna, and the radiation patch is realized by two semicircular patches. The back of the wafer is used as the feed and reflection ground plane of the antenna, and the coupling gap is located directly below the radiation patch, which is used to stimulate the radiation patch. The patch antenna is fed by CPW with terminal open circuit and slot coupling, and the size of CPW is adjusted to make its characteristic impedance 50 Ω, and the function of the coupling gap is to excite the whole patch without an additional gap coupling layer, which makes it easier to integrate with the circuit. It is precisely because of the existence of the coupling gap that the current which originally flows along both sides of the CPW gap on the floor will flow along the edge of the coupling gap, so that the electromagnetic coupling between the CPW and the radiation patch is enhanced. **Fig. 7** is a structural diagram of the slot coupling antenna.



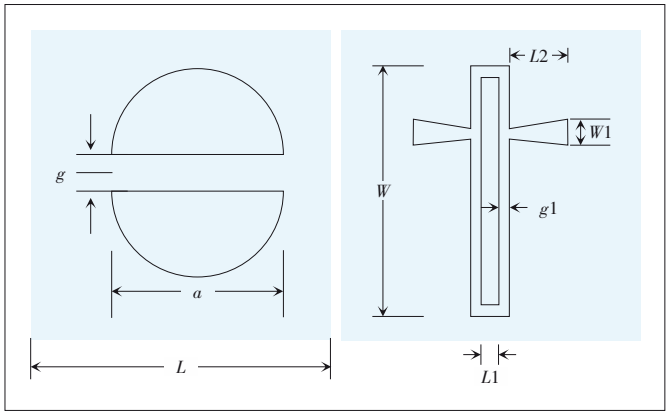
▲ **Figure 6. Comparison between test and simulation results of 3D stacking coplanar waveguide (CPW).**

The electromagnetic simulation software high frequency structure simulator (HFSS) is used to simulate and optimize the slot coupling antenna. After analysis and optimization, the size of the antenna element is 5 mm × 5 mm, the diameter of the two semicircular radiation patches is 1.43 mm, the gap of the two semicircular radiation patches is g=0.196 mm, and the size of the feeder and coupling gap is W=2.8 mm, $W1$=0.2 mm, $L1$=0.07 mm, $L2$=0.615 mm, $g1$=0.025 mm. **Fig. 8** shows the specific structure of the antenna.

The slot coupling antenna is fabricated by wiring the front and back sides of the glass wafer. First, the radiation surface



▲Figure 7. Antenna structure and geometry.



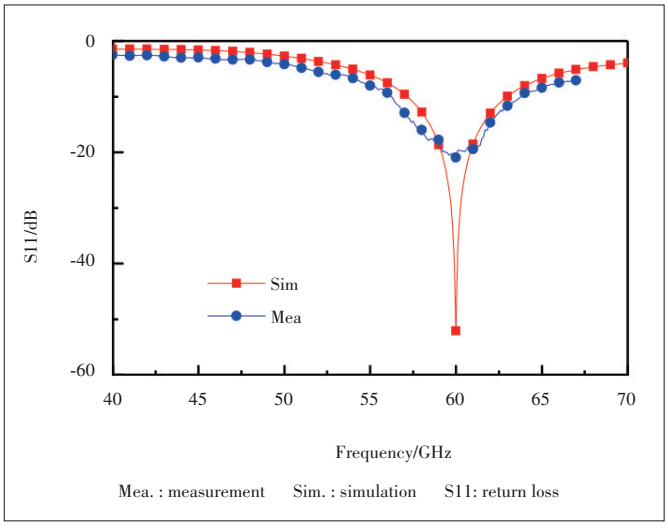
▲Figure 8. Specific structure of the antenna.

of the antenna with 5 μm thick copper is made on the front of the glass wafer, and then it is protected with 10 μm thick polyimide. The CPW feeder and coupling gap are made on the back of the glass wafer, also protected by polyimide, and a rectangular test port is opened on the polyimide layer to leak the copper CPW transmission line.

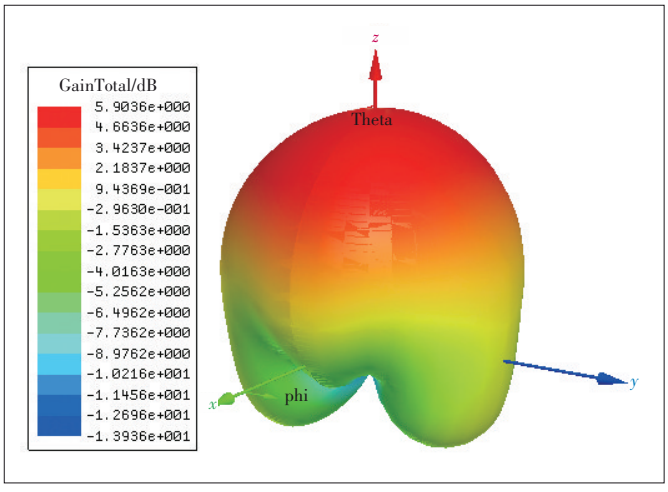
The structure of the antenna is measured by the high frequency probe table. **Fig. 9** shows the slot coupled antenna photos and test photos. From the measurement results, it can be found that the working frequency of the antenna whose reflection coefficient is less than −10 dB is 56.2 – 63.8 GHz. The difference between the simulation results and the measurement results is mainly attributed to the deviation of the process in the manufacturing process, but the antenna still has the working bandwidth of 7 GHz, which meets the design requirements very well. **Fig. 10** shows the emission coefficient of the antenna.

Fig. 11 shows the radiation pattern of the antenna. We can see that the radiation direction of the antenna is directly above the radiation patch, which is very suitable for the stacking integration of RF microsystem and antenna. The top of the 3D stack integration is used for the manufacture of transceiver an-

▲Figure 9. Slot coupled antenna photo and test photo.



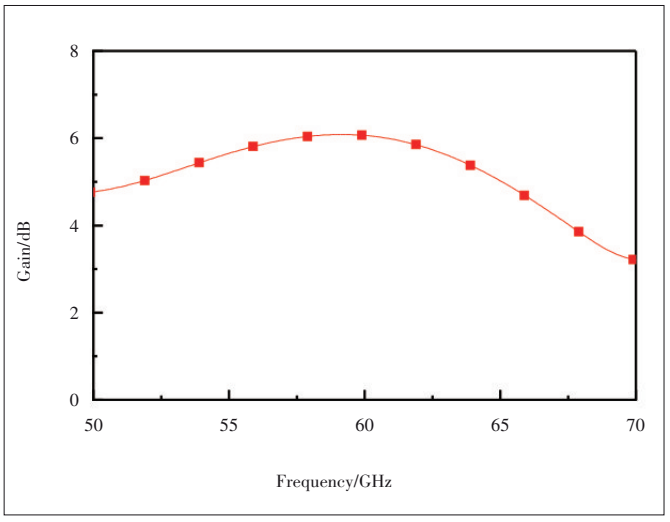
▲Figure 10. Reflection coefficient of antenna.



▲Figure 11. Radiation pattern of antenna.

tennas and the bottom is used for the integration of RF chips.

The gain of the antenna is higher than 5.5 dB in the whole working bandwidth and has the maximum gain of 6 dB in 59.8 GHz. And it has a good directionality. **Fig. 12** shows the simulation results of antenna gain in the working bandwidth.



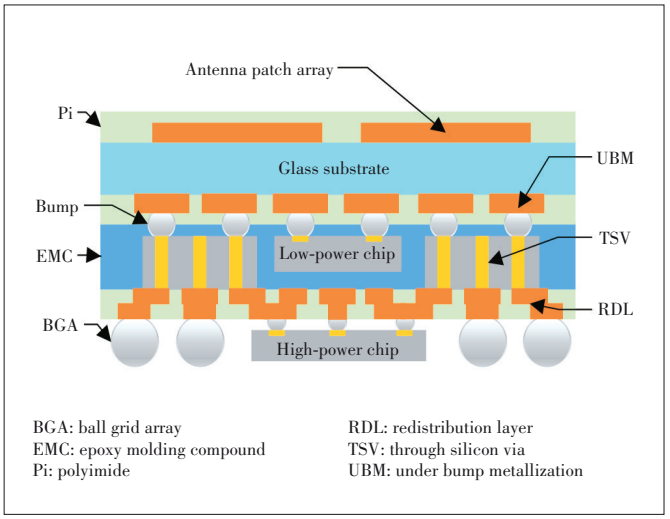
▲**Figure 12. Simulation results of antenna gain in working bandwidth.**

4 Integration of RF Microsystem and Antenna

4.1 Architecture of AiP

In this paper, a specific packaging prototype is made for a 5G communications equipment. It consists of 9 chips and a 64-unit antenna array, including 3 low power RF chips, 2 through silicon via (TSV) transfer chips and 4 high-power chips. The TSV transfer chip is used to realize vertical signal transmission. **Fig. 13** is a schematic diagram of the structure of a 3D fan-out RF microsystem and antenna integrated prototype.

The architecture of AiP is depicted in **Fig. 14.** The RF module demonstrates a multi-layer structure, with antenna and chip layers stacked vertically, and at the very top of the module, the antenna patch array as well as the feeding structure is fabricated on the glass substrate for Tx/Rx channels. As the kernel part, high power chips are embedded in the fan-out (FO) module and interconnected with RDL and TSV structures to establish the transceiver sections; additionally the lower power chips are attached beneath as the signal processing section, thus the solder balls can be arranged on the bottom side as in/out ports. The whole module can be soldered on the system board as an RF transceiver.

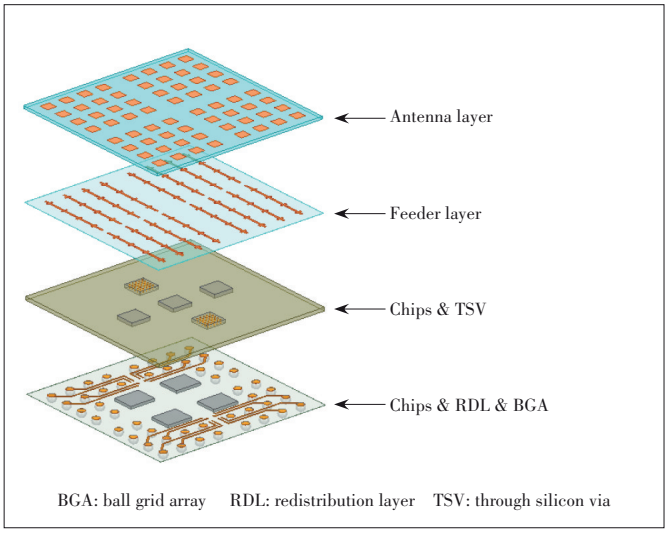


▲**Figure 13. Architecture of integrated prototype of 3D fan-out RF microsystem and antenna.**

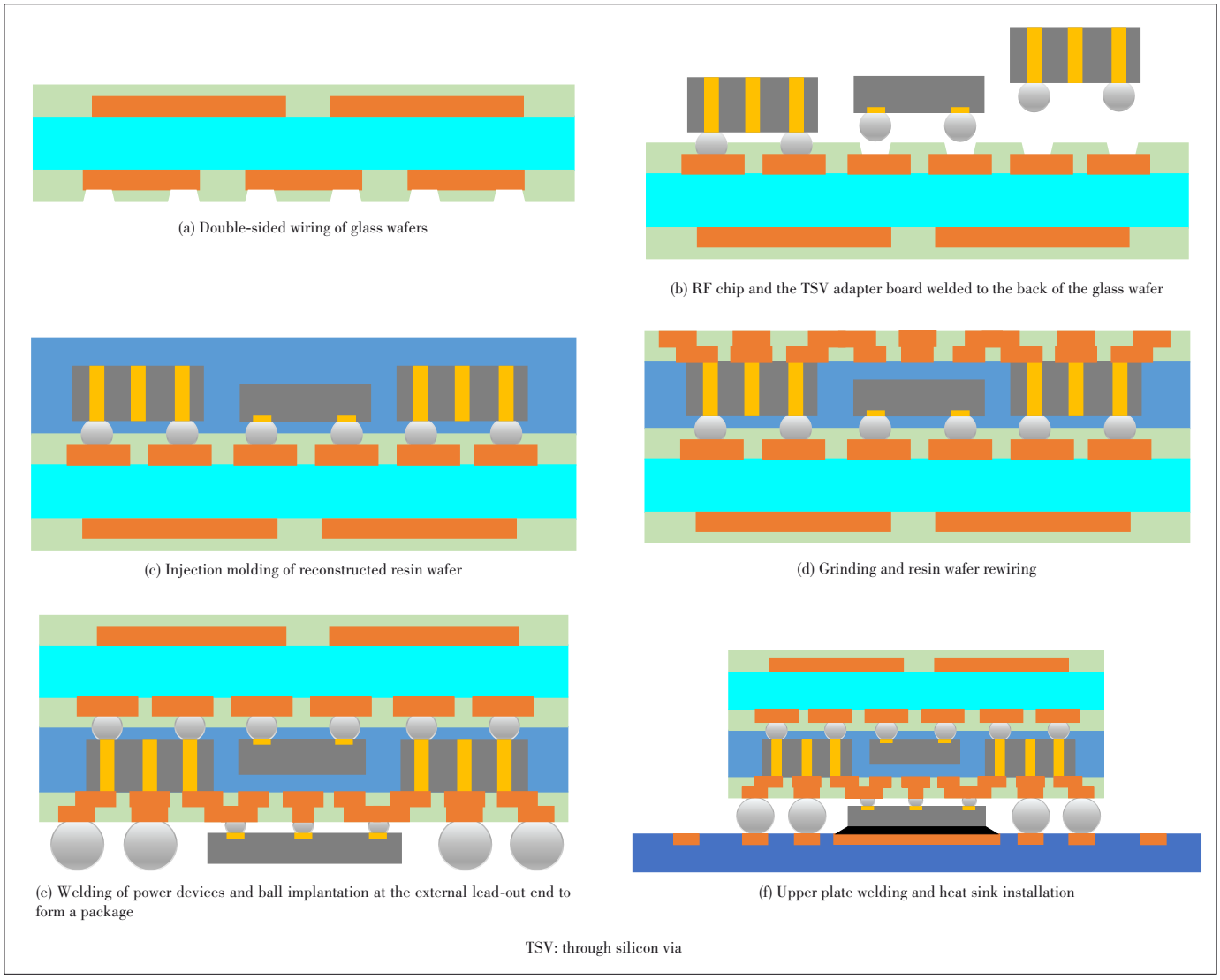
4.2 Fabrication Process of AiP

The integration of RF microsystem and antenna is realized by a new wafer-level 3D fan-out packaging process, different from the traditional 3D stacking packaging. In this paper, a permanent bonding process of resin wafer and glass wafer is adopted, and the BGA welding process is avoided between the two-layer wafers, which is very important for the requirement of low loss of RF devices. The interconnection system of RF devices and antennas is directly realized by RDL process. The wafer-level packaging technology takes the wafer as the processing object and carries out the packaging process directly on the wafer, which has high machining accuracy and consistency, and its wiring accuracy can reach 1 μm. The RF transmission loss of wafer-level packaging verified in the first section above shows that the transmission loss of RF interconnection is very small, which will be very conducive to the integration of RF microsystems and antennas. **Fig. 15** shows the packaging process of the 3D fan-out RF microsystem used in this paper.

The specific fabrication process of the RF micro-system and antenna integrated process prototype is as follows. First, a



▲**Figure 14. 3D fan-out RF microsystem.**



▲**Figure 15. RF microsystem integration process.**

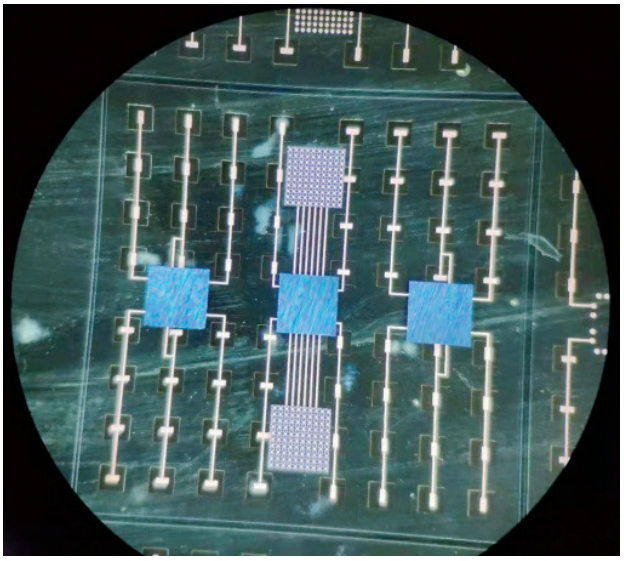
wiring layer and a passivation layer are formed successively on the front and the back of the glass wafer, and the passivation layer is opened on the back of the glass wafer. The TSV transfer chip, the filter and the antenna tuner chip with bump are flip-welded to the opening of the passivation layer on the back of the glass wafer. **Fig. 16** shows a process photo of five chips flip-flopped to the back of the glass wafer.

And then the components such as the TSV transfer chip, the filter and the antenna tuner are coated with coating material to form a reconstructed new wafer carrier, the back of which is thinned to expose the copper column welding disc surface of the TSV adapter plate, and a wiring layer, a passivation layer and a UBM layer are formed on its back. Then the power amplifier, low noise amplifier, transceiver control chip, power management chip and other components are soldered to the UBM layer on the back of the reconstructed new wafer. Solder ball bumps are grown at the UBM layer on the back of the reconstructed wafer carrier to form the final package. The process prototype of the integration of 3D fan-out RF microsystem and antenna is shown in **Fig. 17**.

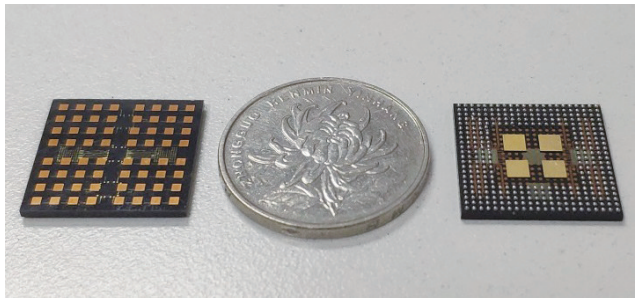
The integrated packaging process scheme of RF microsystem and antenna has the following advantages:

(1) The glass wafer and the resin wafer are bonded together, and there is no need to untie them in subsequent processing and use, which effectively solves the warping problem of the reconstructed wafer and improves the reliability of the product. At the same time, the integration of this process is also promoted.

(2) The processing technology of welding the chip assembly to the glass wafer and then wrapping it with coating material can effectively avoid the chip offset problem caused by the liquefaction flow of coating material and curing process in the traditional coating forming process, and the processing precision is higher. Radio frequency signal transmission loss is lower.



▲Figure 16. Chips welded to the back of the glass wafer.



▲Figure 17. Process prototype of 3D fan-out RF microsystem.

(3) With the technology of wiring on the back of the glass wafer and then reconstructing the wafer with cladding, the double-sided wiring of the reconstructed wafer can be effectively realized, the complex temporary bonding process can be avoided, and the yield and reliability of the product can be improved, thus reducing the difficulty of product processing.

(4) In the final package, the low-power chip assembly is embedded in the coating material, and the high-power chip assembly is welded outside the coating material, which can effectively solve the heat dissipation problem of the high-power chip, and when finally on the board, the back of the high-power chip is coated with a thermal conductive material to connect the chip to the heat dissipation metal surface of the substrate to further improve the heat dissipation performance of the package.

5 Conclusions

In this paper, with 3D fan-out wafer-level rewiring technology, CPW planar transmission lines and stacked CPW transmission structures are fabricated, and the RF transmission performance of CPW is verified. Through the test of CPW transmission line by RF millimeter wave probe, the RF transmission loss of glass wafer in the range of 0 – 67 GHz is obtained. The results show that the RF transmission loss of the glass wafer is only 0.26 dB/mm in 60 GHz, and the loss introduced by the fan-out package is also very small, which indicates that the glass wafer can be used as the packaging substrate of RF devices. Then a slot coupling antenna for 5G communications is fabricated on a 12-inch glass wafer. The antenna works at 56.2 GHz and 63.8 GHz, and the maximum gain of the antenna can reach 6 dB within the working bandwidth. On this basis, an integrated prototype of 3D fan-out RF microsystem and antenna for 5G communications is designed and manufactured, and the prototype is fabricated through the wafer-level fan-out packaging process platform. The process of permanent bonding between the glass wafer and the resin wafer is adopted, and the stacking process of the glass wafer and the resin wafer is avoided in the implementation process. In this way, the package has higher structural strength, higher reliability, less warping and lower process complexity, and shortens the processing cycle. Through the above conclusions, the effectiveness of glass wafer as RF device packaging is verified, and a feasible integrated solution of 3D fan-out micro-system and antenna is provided for 5G communications.

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