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State of the Art in Passive Bandpass Filter Solutions for 60 GHz Communications

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Abstract

This paper reviews the state-of-the-art filter designs for 60 GHz applications. The most promising filter solutions at this frequency include filter-in-package where the filter itself is design in the packaging platform and filter-on-chip which is an on-chip filter co-design for miniaturized system size with low packaging cost. Design methodology, design technology, key performance parameters, similarities and differences, advantages and drawbacks, and future trends are explored and studied. Filters in the printed circuit board (PCB), low temperature co-fired ceramics (LTCC), organic material, and bipolar complementary metal oxide semiconductor (BiCMOS) chips are summarized and compared in details. Future design trends and challenges are also given after the review.

Keywords

60 GHz; bandpass filters; passive; review

1 Introduction

he unlicensed 60 GHz band is a promising solution to future Gb/s wireless communication. It has been a hot research topic in the past decade. To achieve high performance systems, the passive bandpass filter (BPF) plays a critical role in rejecting unwanted interferences or harmonics. For 60 GHz to enter commercial market where the cost and size are mostly concerned, the filters are required to achieve low insertion loss, feasibility of integration, compact size, small form - factor, and mechanical flexibility for bendable electronics.

Researchers have demonstrated many successful implementations of 60 GHz BPFs [1]–[12]. Many technologies have been explored, e.g. the printed circuit board (PCB) technology and low temperature co-fired ceramics (LTCC) technology [1]–[3], targeting for different application scenarios. Some filters have been developed using organic material, which can be bended without sacrificing much of the performance [4]. These filters belong to in-package filters that sit inside the packaging platform. Unlike in-package ones, filters on chip offer a higher level of integration [6]–[12]. However, their performance has to be degraded due to the thin oxide layer in bipolar complementary metal oxide semiconductor (BiCMOS) technologies.

In this paper, we provide a comprehensive overview of filter design progress for 60 GHz applications. With the compiled data and design method, researchers could quickly understand this research area and possibly identify research directions. The results are also tabulated for a clear comparison that serves as benchmark data.

2 Filter-in-Package Solutions

Fig. 1 shows an example of a flip-chip packaged 60 GHz chip with filter-in-package solution. Like other conventional approaches for low RF or a few GHz systems, the in-package filter has been developed for nearly a decade for 60 GHz com-



▲ Figure 1. An example of a flip-chip packaged 60 GHz chip with filter-in-package solution.



State of the Art in Passive Bandpass Filter Solutions for 60 GHz Communications

XU Shanshan, MENG Fanyi, MA Kaixue, and YEO Kiat Seng

Special Topic

munications. With the increase in operation frequency, the dimensions of designed filters shrink proportionally. However, the minimum feature size becomes a fundamental limit for these filters.

In the literature, it is rare to find a transmission line based filter in PCB technology, where the minimum dimension is around 4–8 mil that is difficult for high performance filter design. In LTCC technology, the feature size is normally 2–4 mil, but its multi-layer structure is more suitable for cavity filter designs. Such a filter has low insertion loss with compact size suitable for system integration. Besides PCB and LTCC, organic material is often used for filter designs to meet the flexible or bendable circuit requirement. In addition, a new technology named wafer transfer technology (WTT) uses conventional Rogers substrate with metal and dielectric layers similar to monolithic technology. It allows further reduction in filter size with moderate fabrication cost between complementary metal oxide semiconductor (CMOS) and PCB.

Table 1 gives the summary of filter-in-package solutions. In the following, filter-in-package solutions are discussed according to the adopted technologies.

In [3], a quasi-elliptic 60 GHz filter is designed by stacking dual-mode substrate integrated waveguide (SIW) cavities with a shielding cavity (**Fig. 4**). Two dual-mode SIW cavities were stacked together with a coupling cavity in between results in the four-layer structure. Two Jerusalem cross apertures were defected on the top and bottom layers, while two circle apertures were defected on the middle two layers for coupling purpose. The 60 GHz filter was fabricated using the multilayer LTCC technology with dielectric constant of 7.38 and loss tangent of 0.01. The designed BPF has a center frequency of 60 GHz, a bandwidth of 4.5%, minimum insertion loss of 4.9 (if the loss tangent is 0.0015, insertion loss can be reduced to 1.1 dB), a return loss of 21 dB, and a size of 2.36×2.36×1.1 mm³.

2.3 Flexible Material Based Filter

In [4], a wideband millimeter-wave filter is fabricated on a two-layered (or three layered including cover) flexible PerMX polymer (**Fig. 5**). The PerMX substrate is 50 μ m thick and has a dielectric constant of 3. The three - pole filter is designed based on three half wavelength resonators. The filter is fabricated using PerMX 3050 polymer substrate and 14- μ m thick Per-

2.1 PCB Filters

In [1], a fourth - order 60 GHz BPF based on inverted microstrip gap waveguide was designed and fabricated using PCB technology and Rogers 3003 substrate (**Fig. 2**). The minimum insertion loss of the filter is less than 1.6 dB, and 2 dB in average in the passband. The filter achieves 2 GHz bandwidth at 62 GHz. The 11 mm length filter is embedded within a 10 cm inverted microstrip gap waveguide transition prototype (transition has 1.6 dB loss).

2.2 LTCC Filters

In [2], a narrow-band 60 GHz 3pole BPF based on 3D integrated cavity resonators was proposed (**Fig. 3**). The filter is fabricated using LTCC technology with a dielectric constant of 5.5. The $\lambda_g/4$ slot lines are used for the coupling between resonators. The filter achieves a minimum insertion loss of 2.48 dB at center frequency of 58.7 GHz, a return loss of 16.4 dB, a 3 - dB bandwidth of 1.38% (~0.9 GHz) and a size of around 6.5×3.92 mm².

Table 1. Summary of state-of-the-art filter-in-package solutions

]	Ref.	Technology	3-dB passband (GHz)/FBW (%)	Average insertion loss (dB)	Worst return loss (dB)	Lower stopband attenuation (dB/10 GHz)	Upper stopband attenuation (dB/10 GHz)	Size (mm ²)
	[1]	PCB	61.5-63.5/3.2	2	12	~140	~93	~0.5
	[2]	LTCC	58.3-59.2/1.38	3	12	~250	~300	25.5
	[3]	LTCC	58.7-61.4/4.5	5	15	~57	~32	5.6
	[4]	PerMX polymer	50.7-67.3/28	4.2	13	~17	~14	22.7
	[5]	WTT	52-64/20.7	2.2	7	~1	~0.8	~2.5
		FBW	: frequency widene	d bandwidth	PCB: printed circuit board			

LTCC: technology and low temperature co-fired ceramics WTT: wafer transfer technology

Upper metal plate Upper metal p

▲ Figure 2. Filter in [1]: (a) fourth-order inverted microstrip gap waveguide BPF and (b) a manufactured filter in 10 cm inverted microstrip gap waveguide transition prototype.

Special Topic

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State of the Art in Passive Bandpass Filter Solutions for 60 GHz Communications

XU Shanshan, MENG Fanyi, MA Kaixue, and YEO Kiat Seng







16 ZTE COMMUNICATIONS December 2016 Vol.14 No. S1



▲ Figure 5. Fabricated flexible PerMX substrate embedding filters: (a) PerMX substrate after the separation of Si support wafer and (b) bended PerMX flexible substrate [4].

MX 3014 for cover. The designed filter achieves the minimum insertion loss of 3.8 dB at center frequency 59 GHz, a return loss of better than 13 dB, a 3-dB FBW of 28% and a size of $5.4 \times 4.2 \text{ mm}^2$. PerMX has the advantages of low temperature process (<150° C), mechanical flexibility, bendable, low cost and low dielectric constant, and capability of implementing



State of the Art in Passive Bandpass Filter Solutions for 60 GHz Communications XU Shanshan, MENG Fanyi, MA Kaixue, and YEO Kiat Seng

passive circuits to miniaturized RF SIP.

2.4 WTT Technology Based Filter

In [5], with the unique feature of small dimensions of about a few micrometers, WTT (**Fig. 6**) shows a promising future in solving the poor precision control of the dimension and the roughness of the pattern layer using PCB or thick-film process. Based on WTT, a low-insertion-loss bandpass filter is designed and fabricated at 60 GHz with 3 dB bandwidth of 12 GHz and insertion loss of 1.8 dB. The filter is prefabricated on a Si wafer with 3- μ m-thick Cu and 1KÅ SiN dielectric layer and then is transferred to substrate Rogers RT/Duroid 5880.

3 Filter-on-Chip Solutions

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Merging with 60 GHz RF front-end ICs, the on-chip filter is a promising solution for higher level of system integration compared to its in-package counterpart. **Fig. 7** shows an example of a 60 GHz chip using flip-chip packaging solution, with its 60 GHz filter designed and integrated on the same die. Generally, this filter solution has advantages of small packaged size, low form-factor, high level of integration, and possibility for antenna-on-chip integration. Further, the minimum achievable dimension of metal layers in CMOS technology is ~0.1 μ m, which is far smaller than PCB or LTCC technology. Thus, the impedance control and design uniformity are much enhanced



▲ Figure 6. WTT layer definition of WTT in [5].



▲ Figure 7. An example of a flip-chip packaged 60 GHz chip with filter-on-chip solution.

and reliable. However, due to the lossy silicon substrate and thin dielectric layer in (Bi)CMOS compared to other PCB or LTCC technologies, these filters have poor performance in terms of insertion loss, return loss, and stop-band rejection ratio. Furthermore, the overhead size occupied by the filter potentially increases the fabrication cost of chips.

Special Topic

Table 2 shows the performance of state-of-the-art filters on chips. In general, these filters meet the bandwidth requirement of IEEE 802.11ad standard. The insertion loss is around 3 dB–5 dB in average, while maintaining the return loss better than 8 dB. The stopband attenuation varies much across designs, and is usually worse than in-package filters. However, due to the on-chip technique, the filter size is very compact, resulting in a low form-factor overall packaged dimension of less than 0.2 mm².

It is noteworthy to highlight the following three works:

In [6], the authors proposed the second order 60 GHz BPF based on the folded open loop resonator (OLR) with H-shaped DGS (**Fig. 8**). The OLRs use metal 6 and the bridges use metal 5 to avoid inter-cross of the two OLRs. The filter was fabricated using 0.18 μ m CMOS technology. The measured IL, return loss, centre frequency, and bandwidth are 2.85 dB, 18 dB, 59 GHz and 15.5 GHz with a chip size of 368 × 262 μ m² including pads.

In [7], a low loss and compact filter was proposed using rectangular open-loop resonators with a proposed slotted ground, based on IBM 8RF-DM standard 0.13 μ m CMOS process (**Fig. 9**). The open-loop resonators are designed on the top aluminum metal layer (MA) and the ground plane uses the bottom copper metal layer (M1). The thicknesses for MA and M1 are 4 μ m and 1 μ m, respectively, while the thickness between them is 16.6 μ m. By optimizing the slot on M1 to prevent much more leakage to the lossy substrate, the filter achieves 1 dB bandwidth of 9 GHz with center frequency of 61.5 GHz, and an insertion loss of 1.5 dB, return loss better than 9.2 dB.

In [10], a 60 GHz multi-mode bandpass filter using a sandwich capacitor was implemented in 0.18 μ m BiCMOS technology (**Fig. 10**). The capacitor functions as multi-mode perturbation that controls the stopband. Source/load coupling is used to generate two additional transmission zero point to further improve the stopband rejection. The measured filter features a minimum insertion loss of 4 dB and compact size of 0.16 mm².

4 Future Trends and Design Challenges

The development of millimeter - wave filters is moving towards full on-chip solutions. SOC beam-forming systems better implement non-line-of-sight (NLOS) communications than the conventional point-to-point communication at millimeter-wave frequencies, Considering the huge demand of full SOC beamforming systems [13]–[16], filters with high-level integration tend to be more attractive. In large-scale beam-forming systems especially, the packaging cost of in-packaging filters will

State of the Art in Passive Bandpass Filter Solutions for 60 GHz Communications XU Shanshan, MENG Fanyi, MA Kaixue, and YEO Kiat Seng

▼Table 2. Summary of state-of-the-art filter-on-chip solutions

Ref.	Technology	3 dB Passband (GHz)/FBW (%)	Average insertion loss (dB)	Worst return loss (dB)	Lower stopband attenuation (dB/10 GHz)	Upper stopband attenuation (dB/10 GHz)	Size (mm ²)
[6]	0.18 µm CMOS	51.25-66.75/26	3.2	10	19.5	7.7	0.10
[7]	0.13 µm CMOS	57-66/14.6	3.8	10	41.9	10	0.02
[8]	$0.18 \; \mu \mathrm{m} \; \mathrm{CMOS}$	49-71/36.7	5.4	8	15	25	0.10
[9]	0.18 µm CMOS	43-77/58	4.6	10	5	11	0.18
[10]	$0.18 \; \mu m \; \mathrm{BiCMOS}$	50.5-66/27	5	15	15	8	0.18
[11]	$0.13 \; \mu \mathrm{m} \; \mathrm{CMOS}$	58.2-66.2/13	6.9	9.8	35	30	0.35
[12]	$0.13 \; \mu \mathrm{m} \; \mathrm{CMOS}$	56.2-67.4/18.1	3.9	10	7	11	0.29

BiCMOS: bipolar complementary metal oxide semiconductor FBW: frequency widened bandwidth CMOS: complementary metal oxide semiconductor



▲ Figure 8. Proposed filter and its DGS geometry in [6].



▲ Figure 9. Proposed filter in [7]: (a) top view and (b) ground plane.

become a burden as each of the beam - forming elements requires at least one filter.

However, the existing published works lack of good stopband rejection property, which is essential to at least reject interferences from radar channels at ~40 GHz- 50 GHz and 77 GHz. At these radar frequencies, the signal strength is usually much higher than the 60 GHz communication carrier. Thus, poor rejection leads to possible saturation of input amplifier and malfunction of phase locked-loop due to cross-cou-

pling. The fundamental reason is the low quality-factor of onchip devices, typically around 10–20.

One possible solution is to utilize integrated passive devices (IPD) [17]–[20]. It is a form of separately fabricated devices but integrated with CMOS chip by flip-chip to the CMOS pad opening. The quality factor of such devices is around 100. Therefore, the filter developed in such process is expected to have excellent performance. The current challenges lie in the cost of IPD and flip-chip packaging cost by integrating IPD on-to CMOS chips. The recent work in [21] has demonstrated the concept of using IPD for millimeter - wave applications. With the ever-evolving technologies, there is a great vision for IPD.

5 Conclusions

Simulated

-IS211

GD (2,

80

H=9.65 μm

70

50 60

Frequency (GHz)

(b)

40

In the paper, we reviewed several recently published 60 GHz BPFs. The technology comparision shows that all filter designs are towards a lower fabrication cost and compact size. PCB or LTCC based filters have good insertion loss and return loss. However, the 60 GHz systems using PCB or LTCC filters have the size limited by filter sizes due to the lack of integration capability. In addition, most of the filters using PCB or

0.20

0.18

0.16

0.14

0.12

0.10

0.08

0.06

0.04

0.02

-0.02

100 110

(ns)

Group delay

Simulated

IS211

H=8 μm

90

LTCC are narrow band filters with FBW less than 5% . Technologies like WTT and new material like PerMX polymer are adopted to widen the bandwidth. This however sacrifice the filter selectivity, which is an important factor for filters especially when applied to the OOK transceiver. Due to the advancement of CMOS technologies, the performance of CMOS filters have been improved tremendously over the



Measured

- IS11I

IS211

• GD (2,1)

-5

-10

-15

-20

-25

-30

-40

0 10 20 30

S211 & IS111 (dB)

(a)

¹⁸ **ZTE COMMUNICATIONS** December 2016 Vol.14 No. S1



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State of the Art in Passive Bandpass Filter Solutions for 60 GHz Communications

XU Shanshan, MENG Fanyi, MA Kaixue, and YEO Kiat Seng

years. Its insertion loss, however, is still too poor to be used in systems. To achieve both high-level integration and high performance, IPD is a potential solution in the future.

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YEO Kiat Seng (kiatseng_yeo@sutd.edu.sg) received the BEng (EE) in 1993, and PhD (EE) in 1996 both from NTU. He is now Associate Provost (International Relations and Graduate Studies) at Singapore University of Technology and Design (SUTD) and a member of Board of Advisors of the Singapore Semiconductor Industry Association. Dr. YEO is Fellow of IEEE and a widely known authority in lowpower RF/mm-wave IC design and a recognized expert in CMOS technology. He has secured over S\$30M of research funding from various funding agencies and the industry in the last 3 years. Before his new appointment at SUTD, he was Associate Chair (Research), Head of Division of Circuits and Systems and Founding Director of VIRTUS of the School of Electrical and Electronic Engineering at NTU. He has published six books, five book chapters, over 400 international top-tier refereed journal and conference papers and holds 35 patents. Dr. Yeo served in the editorial board of IEEE Transactions on Microwave Theory & Techniques and hold/held key positions in many international conferences as Advisor, General Chair, Co-General Chair and Technical Chair. He was awarded the Public Administration Medal (Bronze) on National Day 2009 by the President of the Republic of Singapore and was also awarded the distinguished Nanyang Alumni Award in 2009 for his outstanding contributions to the university and society.

December 2016 Vol.14 No. S1 ZTE COMMUNICATIONS 19